

# DESIGN OF NEGATIVE CLAMPER

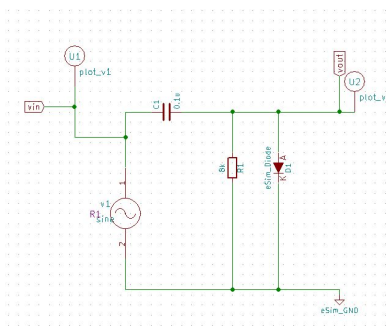
## INTRODUCTION :

A Negative Clamper circuit is one that consists of a diode, a resistor and a capacitor and that shifts the output signal to the negative portion of the input signal. During the positive half cycle, the capacitor gets charged to its peak value  $v_m$ . The diode is forward biased and conducts. During the negative half cycle, the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0 = V_i + V_m$$

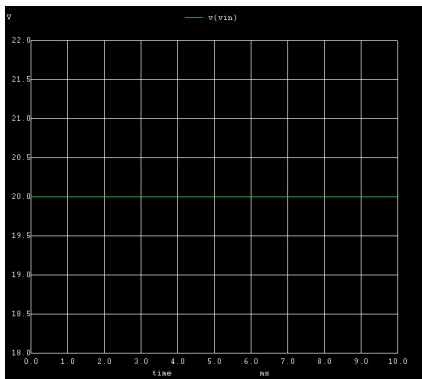
Hence the signal is negatively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

## SCHEMATIC CIRCUIT DIAGRAM:

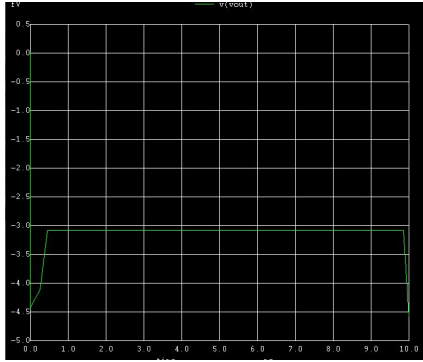


## NGSPICE PLOT:

### INPUT:

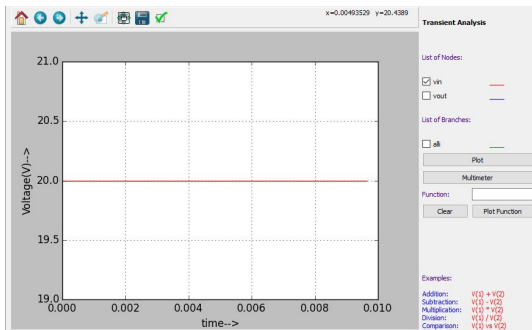


### OUTPUT:

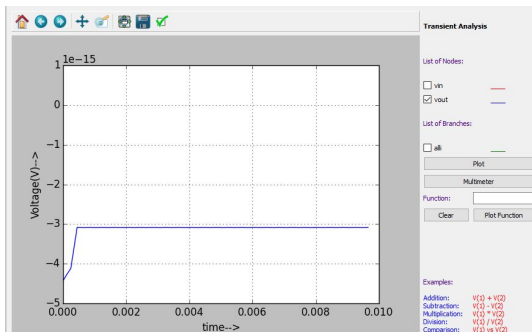


## PYTHON PLOT:

## INPUT PLOT:



## OUTPUT PLOT:



## REFERENCE:

[https://www.tutorialspoint.com/electronic\\_circuits/electronic\\_clamper\\_circuits.htm](https://www.tutorialspoint.com/electronic_circuits/electronic_clamper_circuits.htm)

