CARRY LOOKAHEAD ADDER USING eSim

THEORY: A **carry- lookahead adder** (**CLA**) or **fast adder** is a type of adder used in digital logic. A carry-lookahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, *ripple carry adder* for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry bit have been calculated to begin calculating its own result and carry bits . The carry-lookahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits of the adder.

If we define two variables as carry generate Gi and carry propagate Pi then,

$$P_i = A_i \oplus B_i$$

$$Gi = Ai\ Bi$$

The sum output and carry output can be expressed as

$$Si = Pi \oplus Ci$$

$$C\ i +1 = Gi + Pi\ Ci$$

Where Gi is a carry generate which produces the carry when both Ai, Bi are one regardless of the input carry. Pi is a carry propagate and it is associate with the propagation of carry from Ci to Ci +1.

CALCULATION: A0 A1 A2 A3

\+ B0 B1 B2 B3

S0 S1 S2 S3 C4

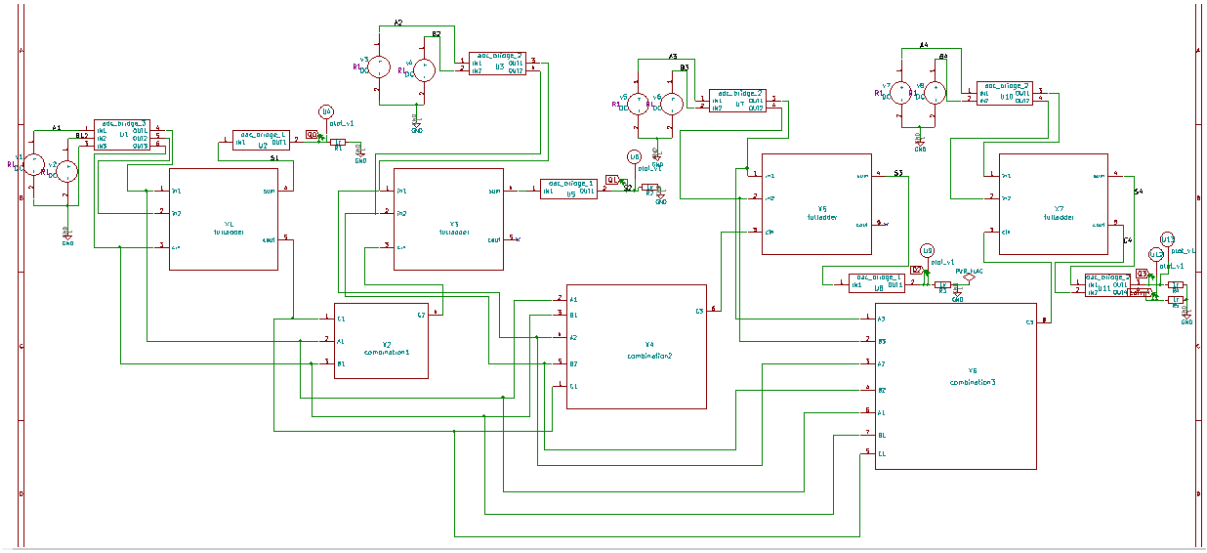
Cin=0; C2=P1C1+G1, C3=P1P2C1+P2G1+G2 , C4=P3P2P1C1+P3P2G1+P3G2+G3

Eg:v1=5 v2=0 v3=5 v4=0 v5=5 v6=0 v7=5 v8=5

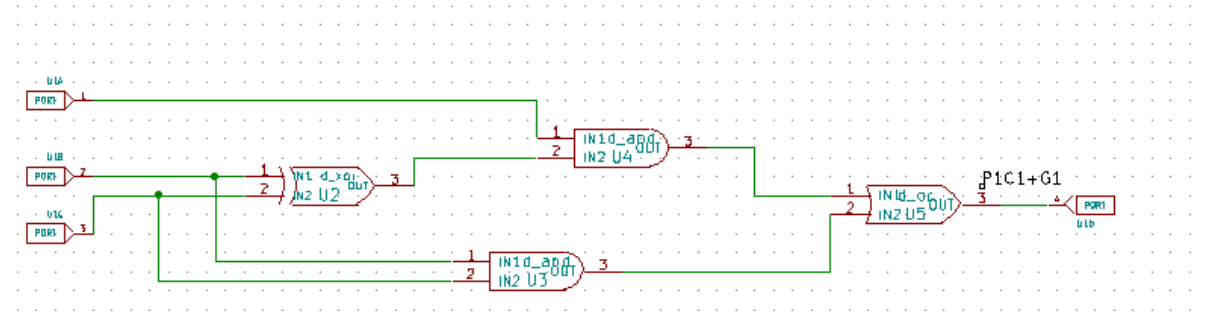
Q0=5 Q1=5 Q2=5 Q3=0 carry(4)=5

SCHEMATIC DIAGRAM:

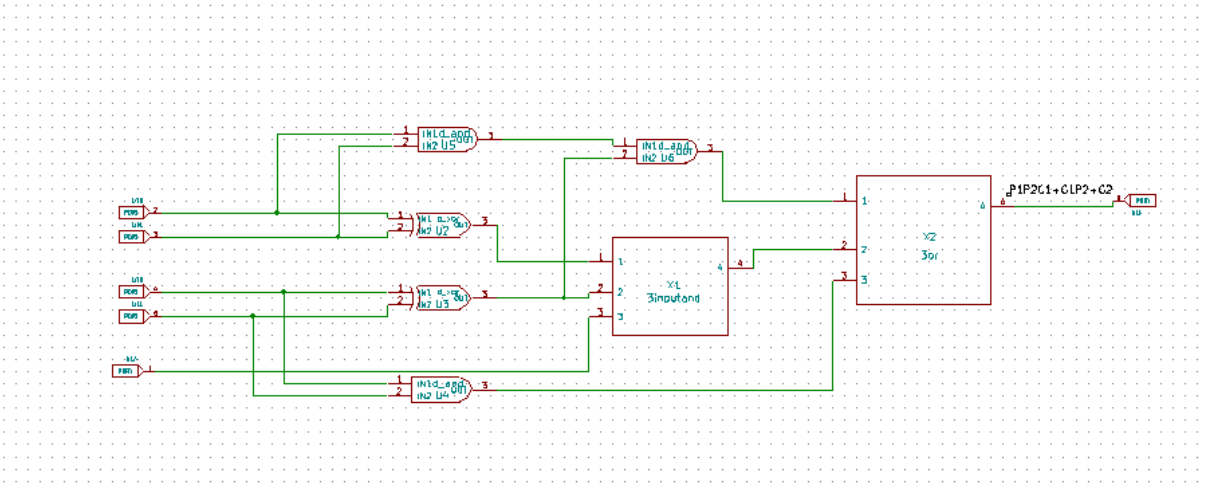
The circuit schematic of carry lookahead adder using eSim is shown below:



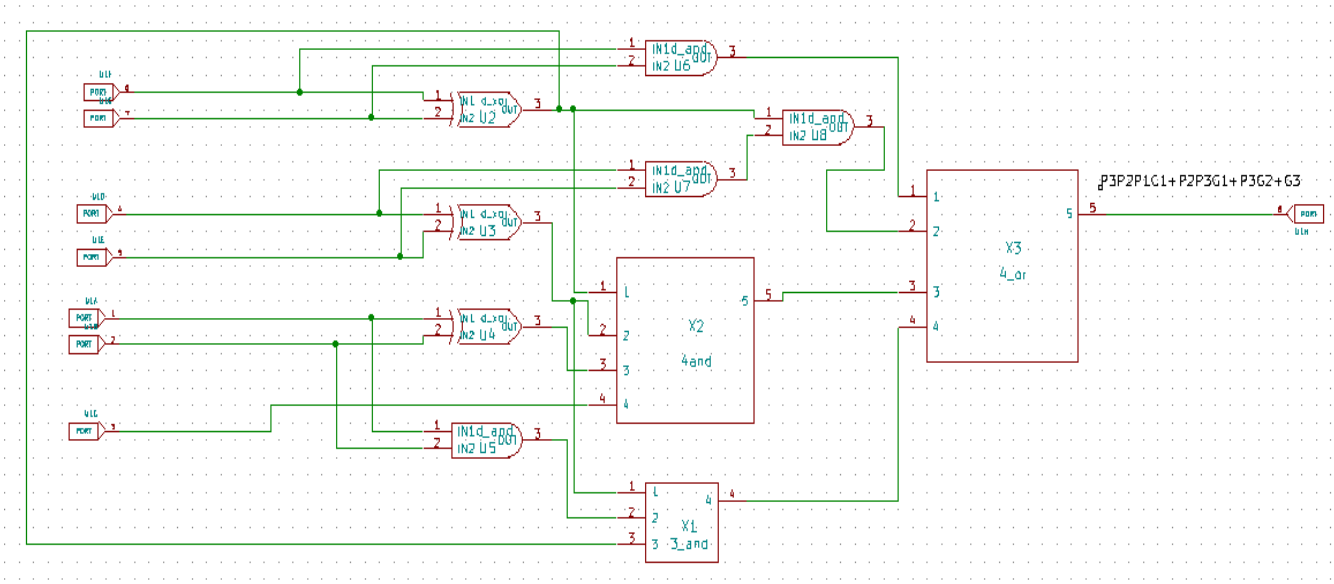
COMBINATION1 SUBCIRCUIT:



COMBINATION2 SUBCIRCUIT:



COMBINATION3 SUBCIRCUIT:



SIMULATION RESULTS:

1.ngspice plots

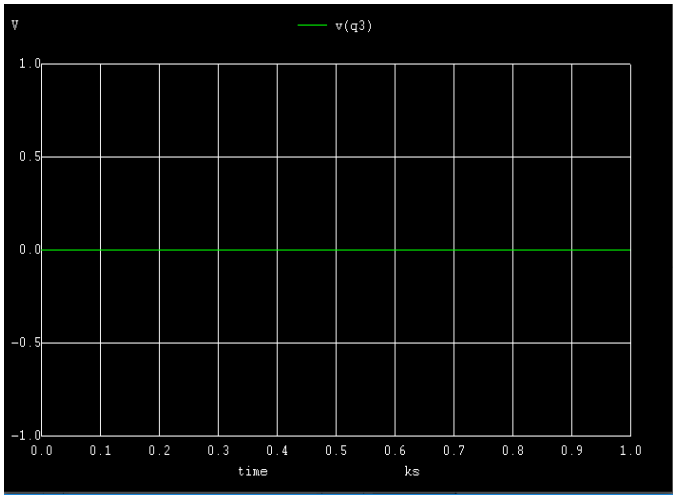


Fig 1:ngspice output plot for q3

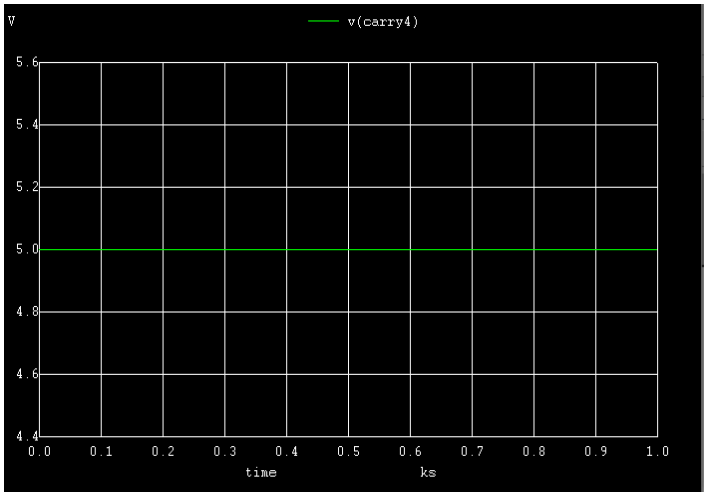


Fig 2:ngspice output plot for carry(c4)

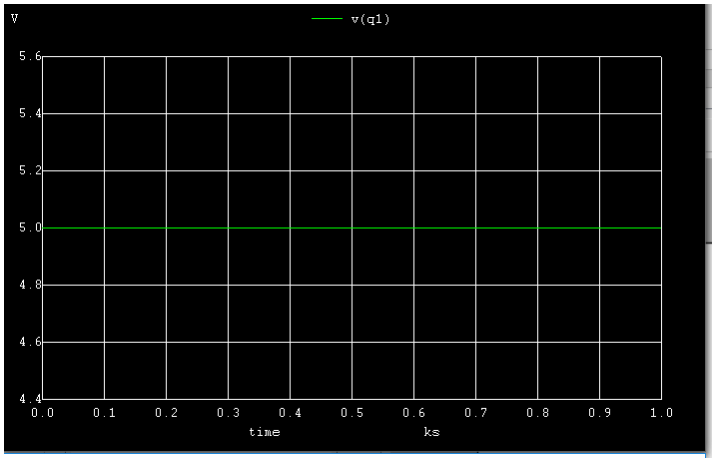


Fig 3:ngspice output plot for q1

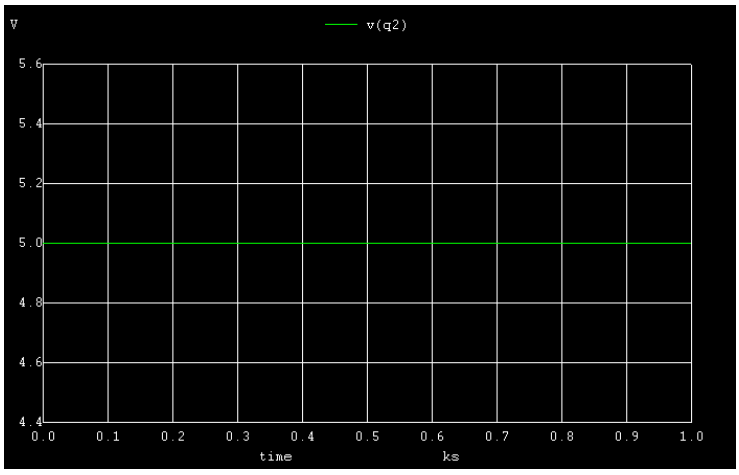


Fig 4:ngspice output plot for q2

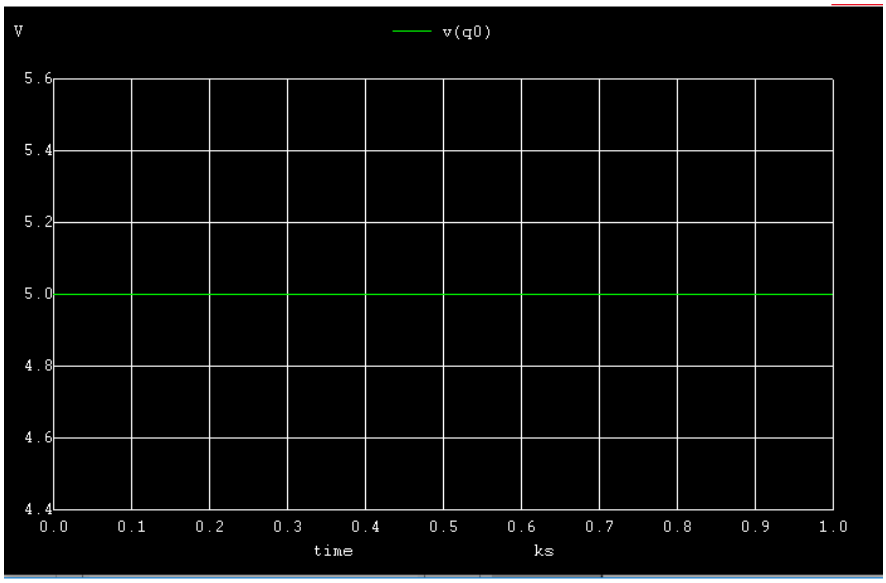


Fig 5:ngspice output plot for q0

2:Python plots

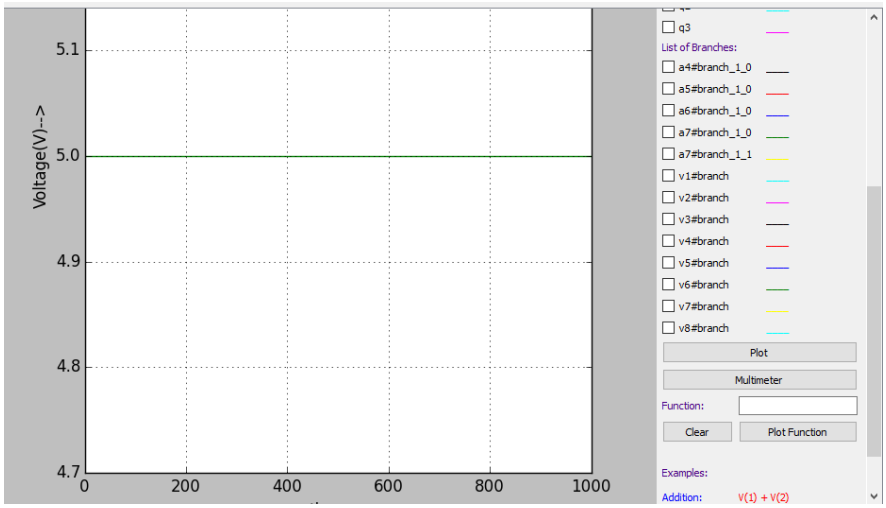


Fig 6:python output plot for q0

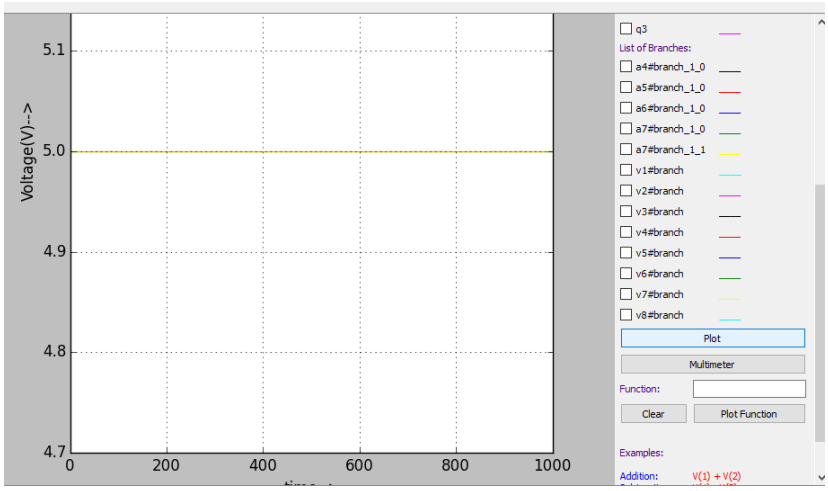


Fig 7:python output plot for q1

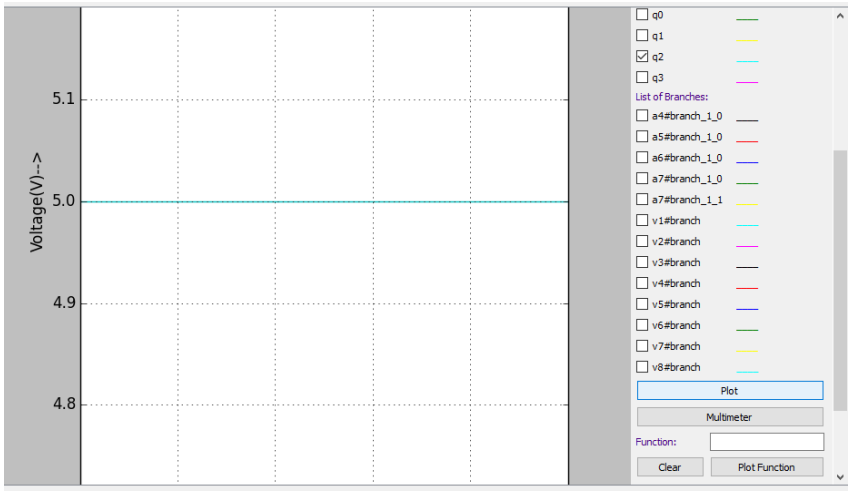


Fig 8:python output plot for q2

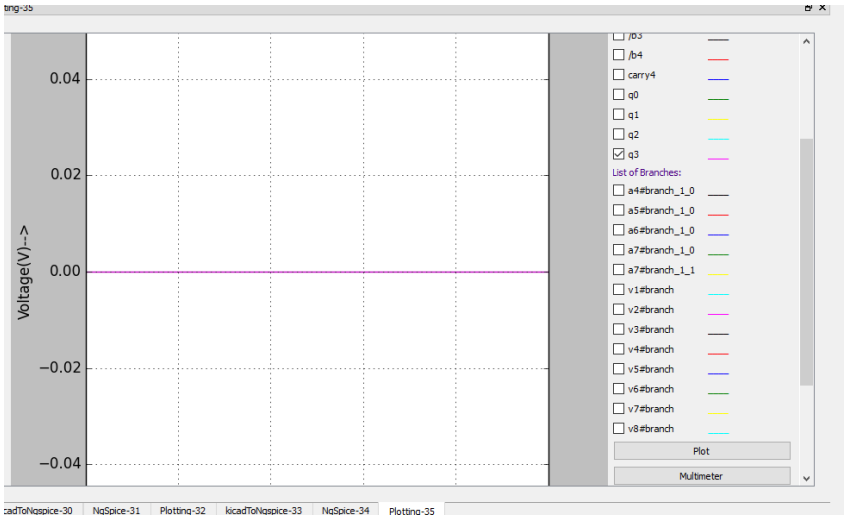


Fig 9:python output plot for q3

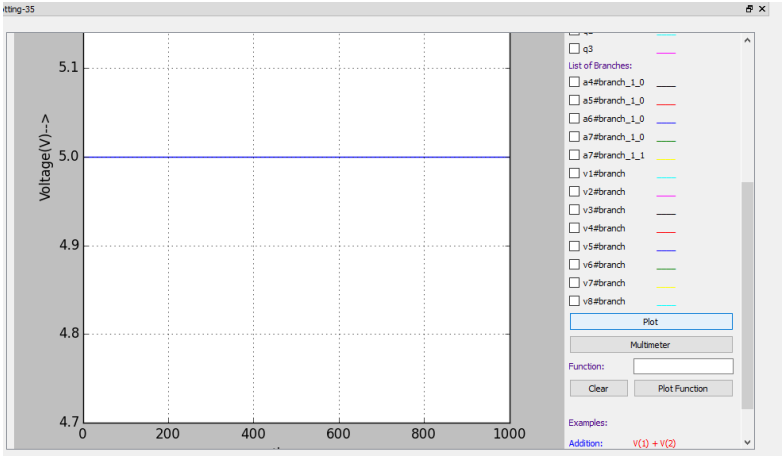


Fig 10:python output plot for carry (c4)

REFERENCE:

https://www.electronicshub.org/carry-look-ahead-adder/

https://en.wikipedia.org/wiki/Carry-lookahead_adder