TITLE OF THE EXPERIMENT

ANALYSIS OF POSITIVE CLAMPING CIRCUIT

THEORY

The need for a clamper circuit is similar to in TV receivers; ; where the signal moves through the capacitive coupling network, and then the DC component of these signals is lost. This DC component (not the same as the one lost) will be reset using the clamping circuits. A clamping circuit restores the DC level. When the negative peak of the signal is raised above zero level, the signal is said to be positively clamped. Here; when the signal is moved to the top or the positive side, both a negative peak and a zero level will meet, called a positive clamper circuit (Figure 1).

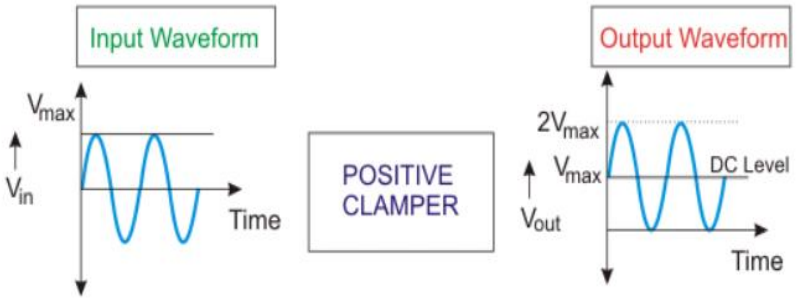

Figure 1. Block diagram of a Positive Clamper Circuit

Principle of Operation of Clamping Circuit

Generally, the clamper circuit depends on the variation in the capacitor time constant as given in equation 1.

$$\tau = RC \qquad (1)$$

The time constant must be sufficient to ensure that the capacitor voltage does not discharge substantially throughout the non-conducting diode. One must choose the values of capacitance and resistance to keep the circuit time constant. The resistance value must be high enough to prevent the rapid discharge of the capacitor. For the duration of diode conduction, the capacitor charging should be very fast. For this, we select a small value of the capacitor.

The C in the positive clamp charges quickly throughout the first negative phase of the AC input voltage. When V_{in} + ve, C is a voltage doubled and V_{in} is -ve, C acts as a battery with a voltage. Thus, we can conclude that the capacitor and the input voltage work against each other. This results in zero net voltage as seen by the load.

DESIGN AND CIRCUIT DIAGRAM

A positive clamper circuit consists of a diode, a resistor and a capacitor and converts the output signal to the positive portion of the input signal. The figure below illustrates the construction of a positive clamper circuit. The positive clamper circuit is shown in Figure 2.

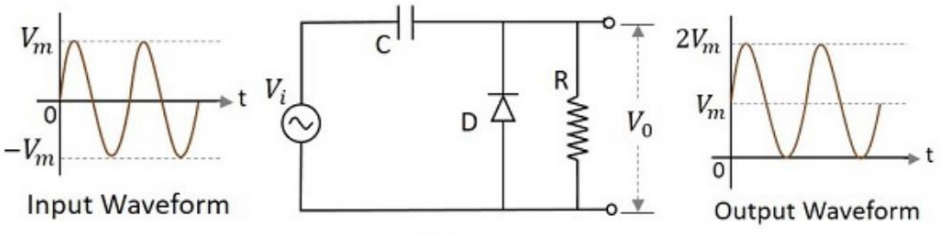

Figure 2.A positive clamper circuit

When the input is initially supplied, the capacitor is not yet charged and the diode is reverse biased. No output is considered at this time. During the negative half cycle, at the peak value, the capacitor is negatively charged on one plate and positive on the other. The capacitor is now charged to its peak value Vm. The diode is forward biased and conducts heavily. During the next positive half cycle, the capacitor is charged to positive Vm while the diode gets reverse biased and gets open circuited. The output of the circuit at this moment will be

$$V_0 = V_i + V_m$$

Hence the signal is positively clamped as shown in the above figure. The output signal changes according to the changes in the input, but shifts the level according to the charge on the capacitor, as it adds the input voltage.

Positive Clamper with Positive Vr

A Positive clamper circuit if biased with some positive reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

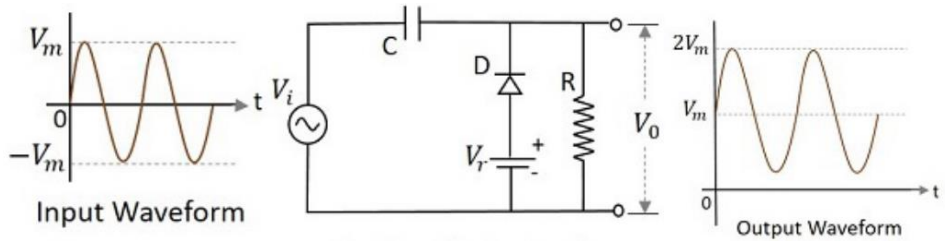

Figure 3.A positive clamper circuit with Positive Vr

During the positive half cycle, the reference voltage is applied through the diode at the output and as the input voltage increases, the cathode voltage of the diode increase with respect to the anode voltage and hence it stops conducting. During the negative half cycle, the diode gets forward biased and starts conducting. The voltage across the capacitor and the reference voltage together maintain the output voltage level.

Positive Clamper with Negative Vr

A Positive clamper circuit if biased with some negative reference voltage, that voltage will be added to the output to raise the clamped level. Using this, the circuit of the positive clamper with positive reference voltage is constructed as below.

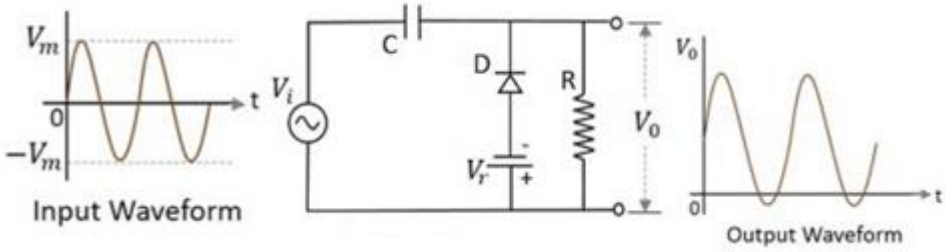

Figure 3.A positive clamper circuit with Negative Vr

During the positive half cycle, the voltage across the capacitor and the reference voltage together maintain the output voltage level. During the negative half-cycle, the diode conducts when the cathode voltage gets less than the anode voltage. These changes make the output voltage as shown in the above figure.