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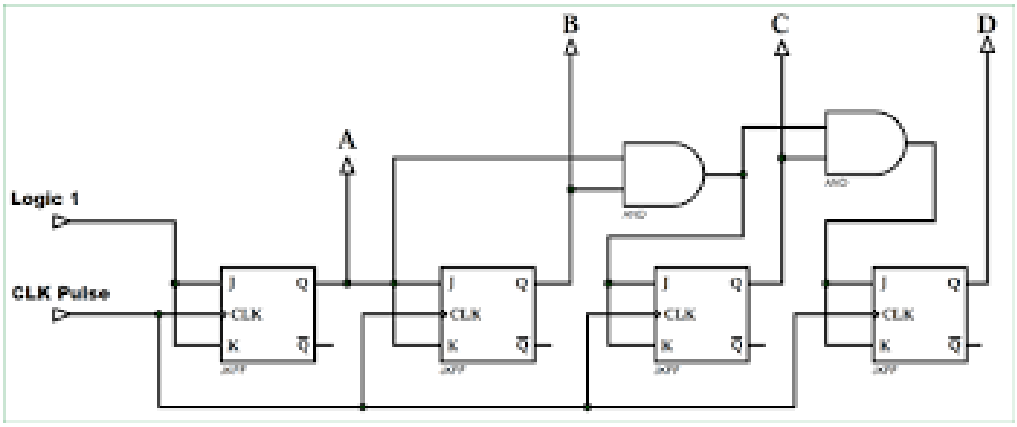
Title :4 BIT SYNCHRONOUS UP-COUNTER

Abstract :

1. A 4-bit Synchronous up counter starts its counting sequence from 0000 in binary i.e 0 in decimal and increment in upward counting sequence by "one" for each clock pulse until it count upwards to 1111 in binary i.e 15 in decimal and then restart new counting cycle by getting reset itself from 0000 again. An external clock pulse are provide directly to each of the J-K flip-flops in the counter. The first flip-flop, flip-flop FFA (LSB) are connected to HIGH signal, logic "1" allowing the flip-flop to toggle on every clock pulse. Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse. The J and K inputs of flip-flop FFB are connected directly to the output QA of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage. These additional AND gates generate the required logic for the JK inputs of the next stage. If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time. Then as there is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit. Because this 4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111). Therefore, this type of counter is also known as a 4-bit Synchronous Up Counter. However, we can easily construct a 4-bit Synchronous Down Counter by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above. Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again. Using esim the circuit is simulated by step by step process: 1.Create a schematic for the selected project or open existing schematic associated with the project. 2. Specify start time, step time and stop time for simulation. Also for specifying supply voltage. And convert into NGSpice model. 3.Simulate the schematic.4. Click "New Project" and type project name of choice and click "OK". This will create a new project in Projects plane. 4. Double click on project name to select it. In console window it should say your project is current project. Click on Create Schematic icon to start creating the project schematic.5. Wire tool – used to connect components. 6.Label tool – used to create labels which can then be connected to probes to label what quantity that probe is measuring.7.Annotate tool. 8.Electrical rules check – checks whether all connections are proper and if any component is left unconnected.9.Generate netlist tool – To generate Pspice netlist which can then be simulated.

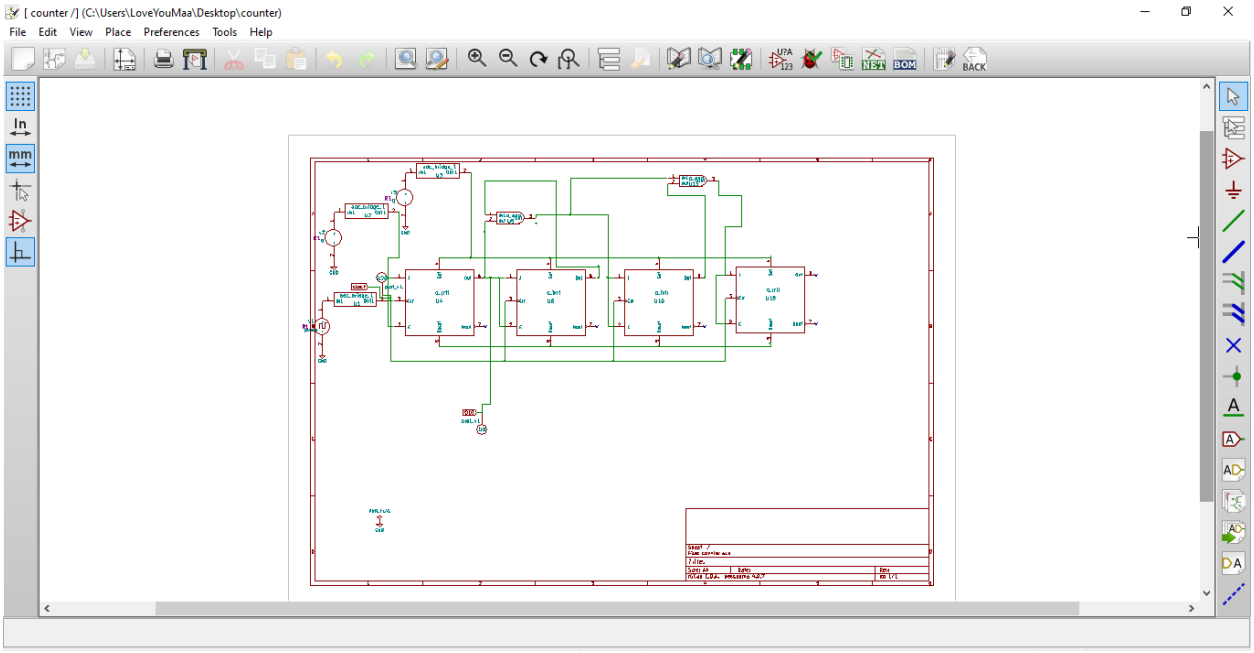
Circuit Diagram:

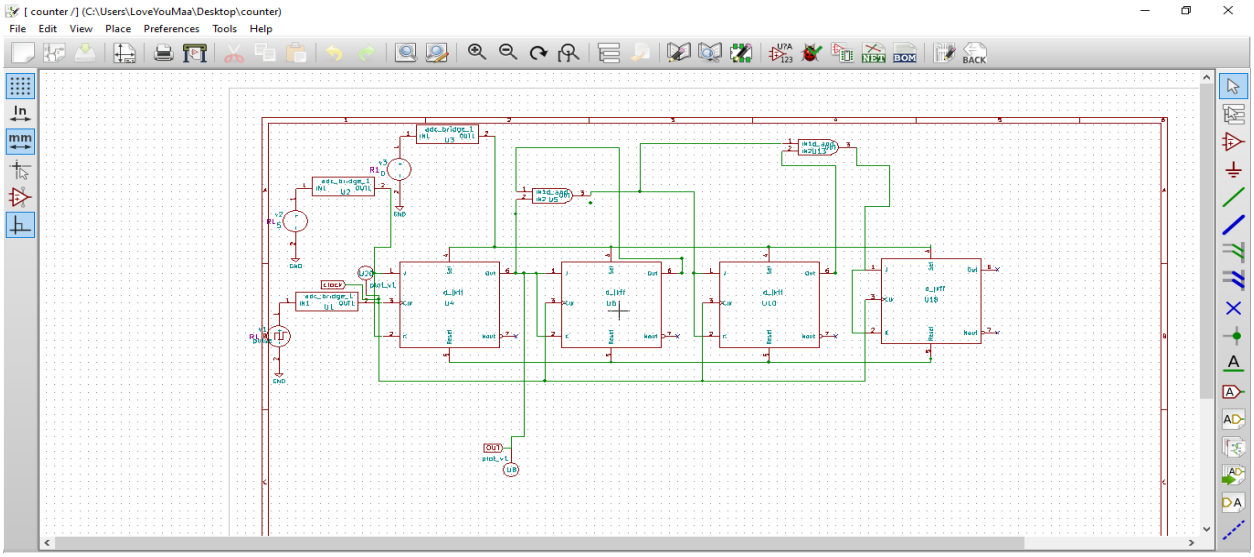


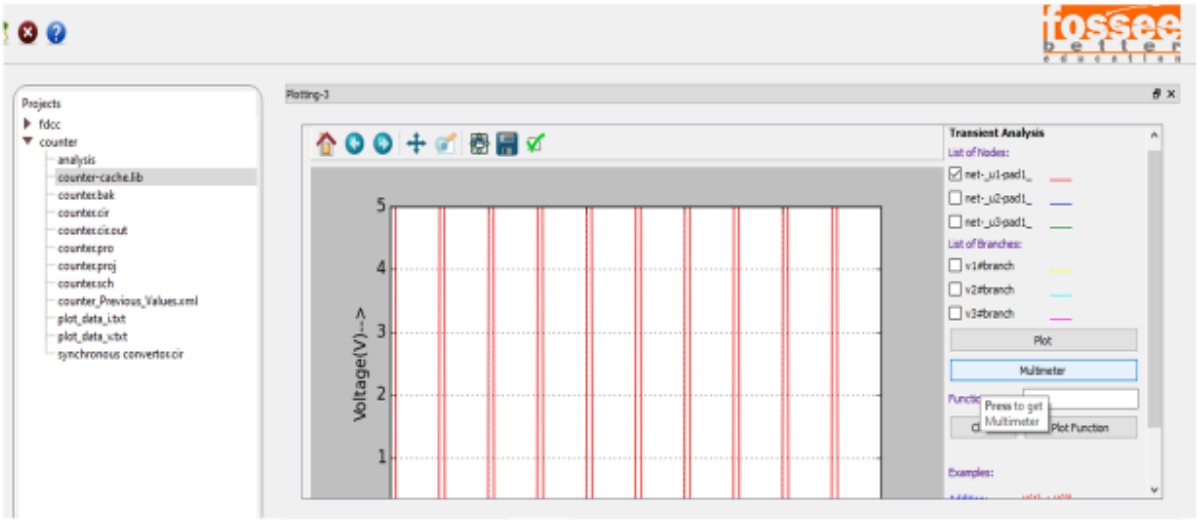
ESIM Required Components:

Synchronous up counter	
Component Name	**Type**
d_jkff	j-k flip flop
clock	clock input
d_and	and gate
dc	dc voltage source for logic 1

ESIM Circuit design snapshot:







In plotting window, you can tick which nodes to plot and click on "Plot" button