4:16 de multiplexer using eSim

THEORY: A de multiplexer (or de mux) is a device that takes a single input line and routes it to one of several digital output lines. A de multiplexer of 2^n outputs has n select lines, which are used to select which output line to send the input. A de multiplexer is also called a data distributor.

De multiplexers can be used to implement general purpose logic. By setting the input to true, the de mux behaves as a decoder.

The reverse of the digital de multiplexer is the digital multiplexer

TRUTH TABLE:

INPUTS				OUTPUTS															
A	B	C	D	X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{10}	X_{11}	X_{12}	X_{13}	X_{14}	X_{15}
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

CALCULATION:

Eg:v0(S0)=5 v1(S1)=5 v2(S2)=0 v3(S3)=5

5055->1011->11(decimal)

q0=0 , q1=0, q2=0, q3=0, q4=0, q5=0, q6=0, q7=0, q8=0, q9=0, q10=0, q11=5, q12=0, q13=0, q14=0, q15=0

SCHEMATIC DIAGRAM

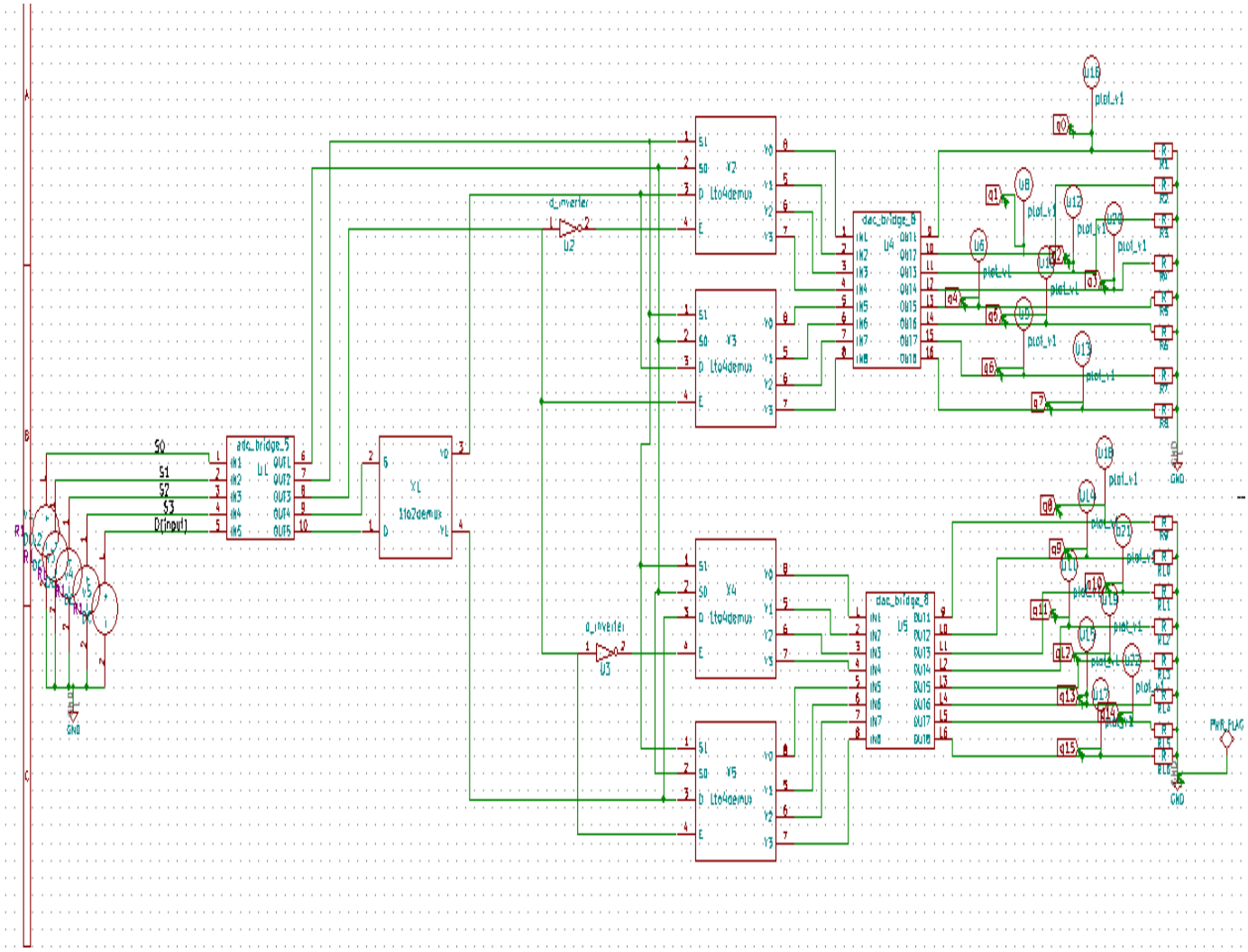

Fig 1:`1 to 16 de multiplexer circuit diagram

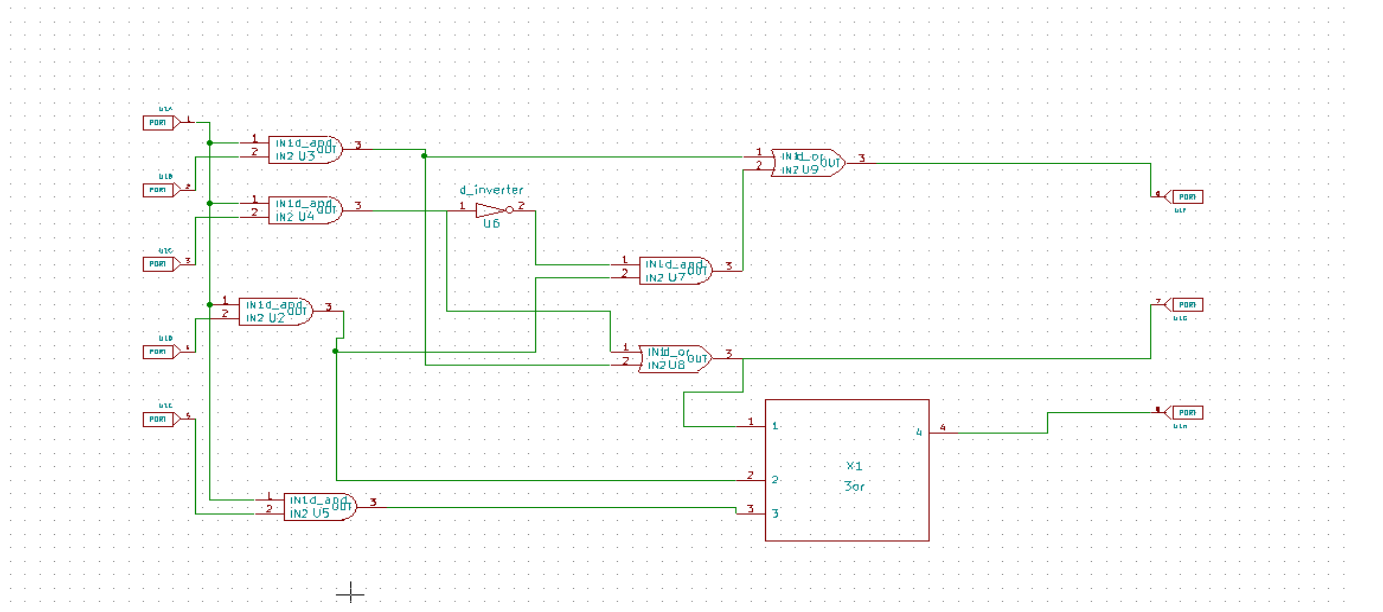

Fig 2:1 to 4 de multiplexer circuit diagram(Subcircuit)

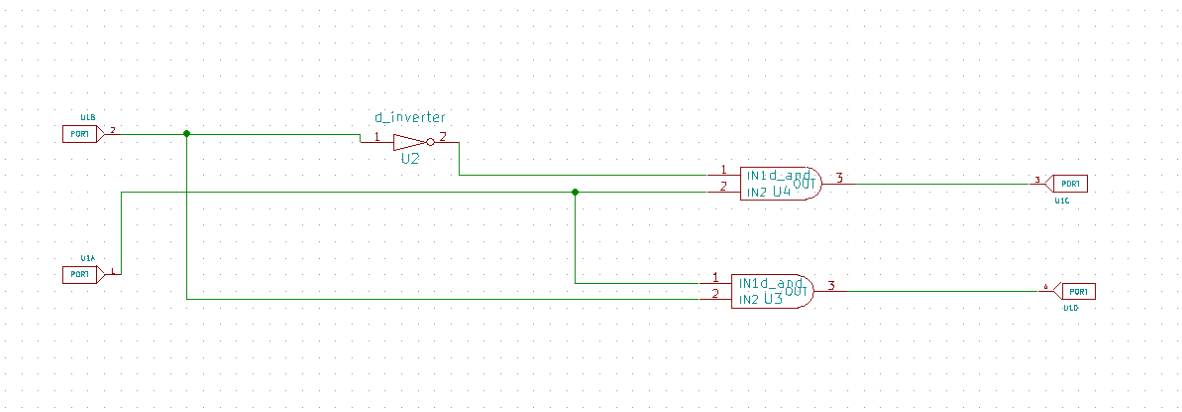

Fig3:1 to 2 deultiplexer circuit diagram(Subcircuit)

NgSpice Plots:

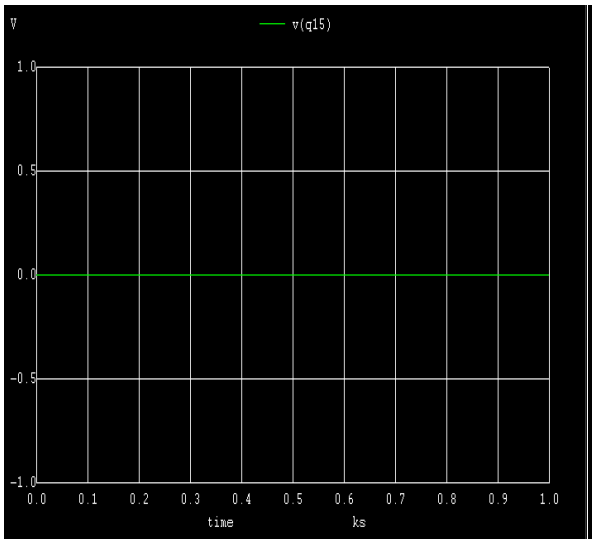

Fig1:q15 output plot

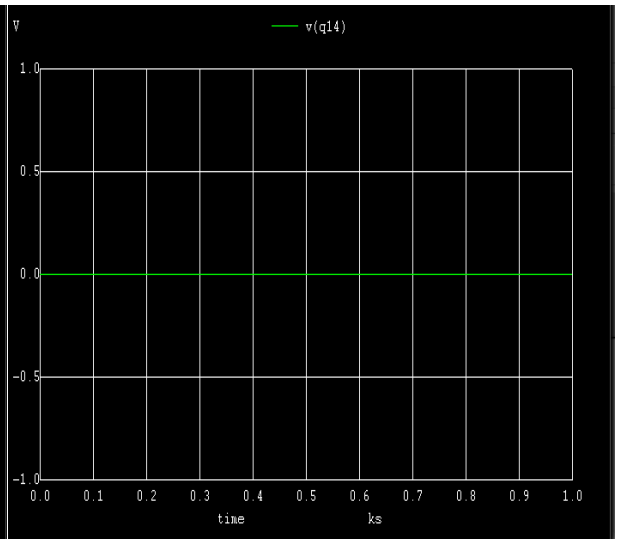

Fig2:q14 output plot

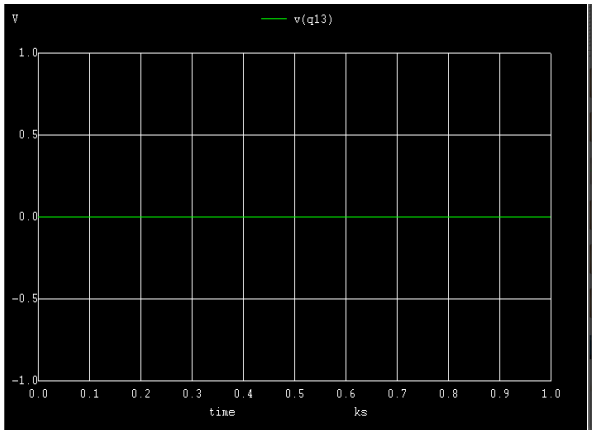

Fig3:q13 output plot

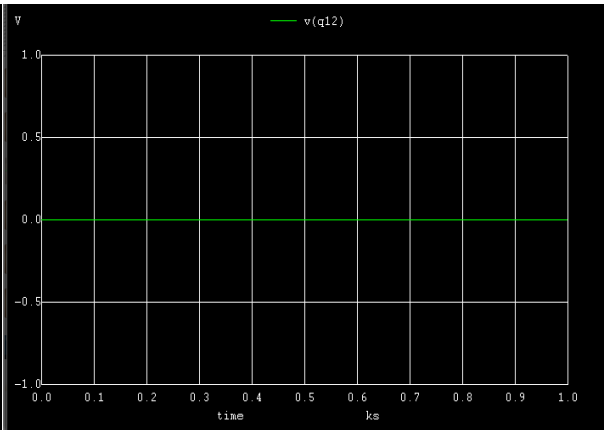

Fig4:q12 output plot

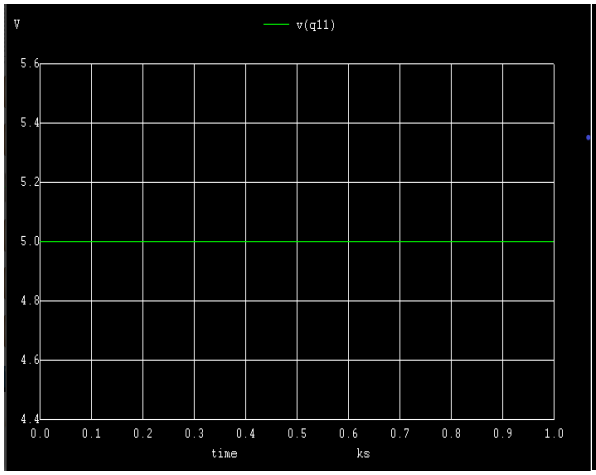

Fig5:q11 output plot

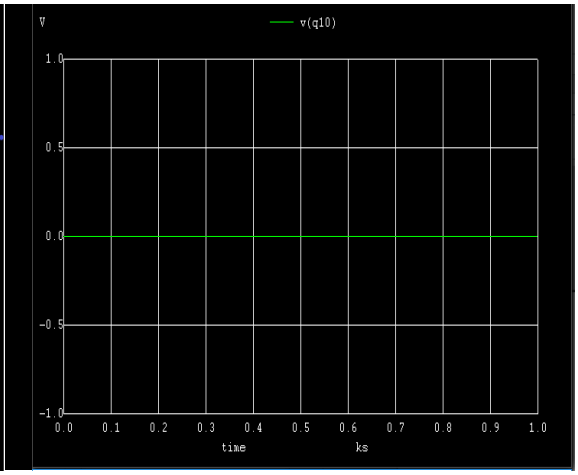

Fig6:q10 output plot

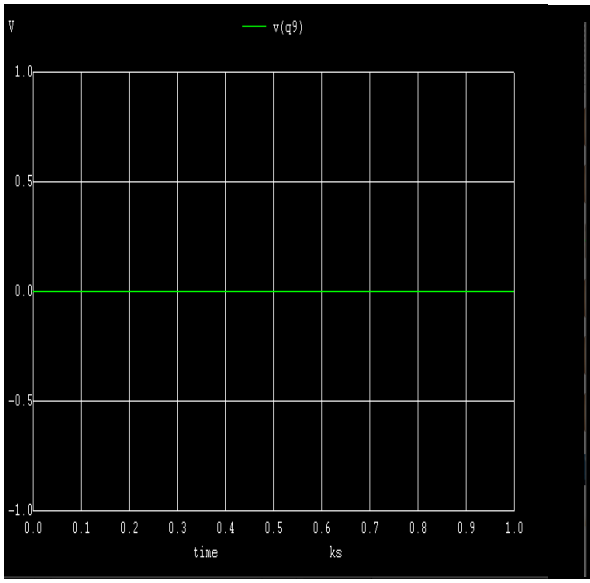

Fig7:q9 output plot

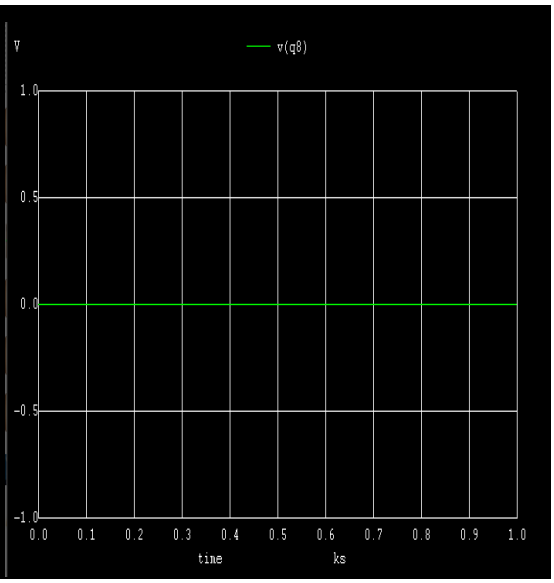

Fig8:q8 output plot

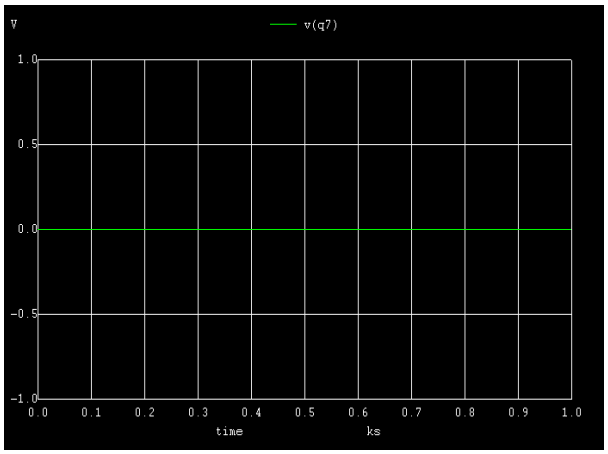

Fig9:q7 output plot

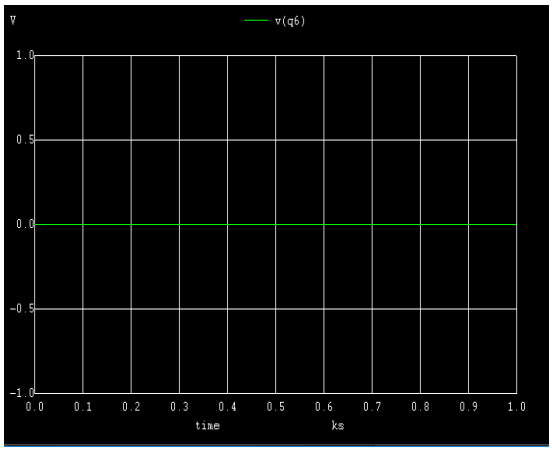

Fig10:q6 output plot

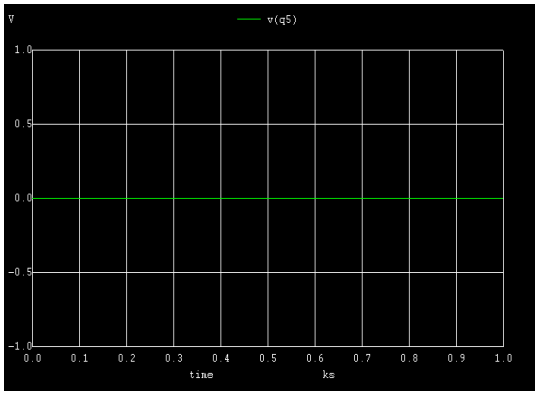

Fig11:q5 output plot

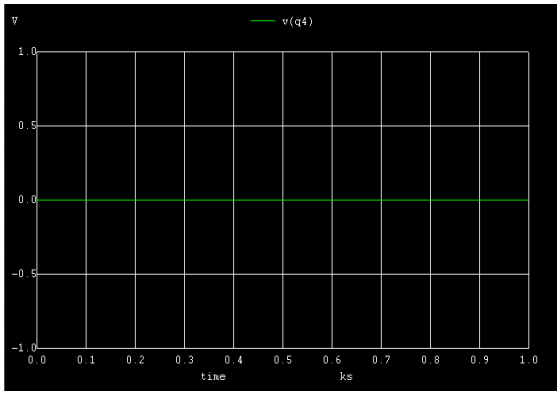

Fig12:q4 output plot

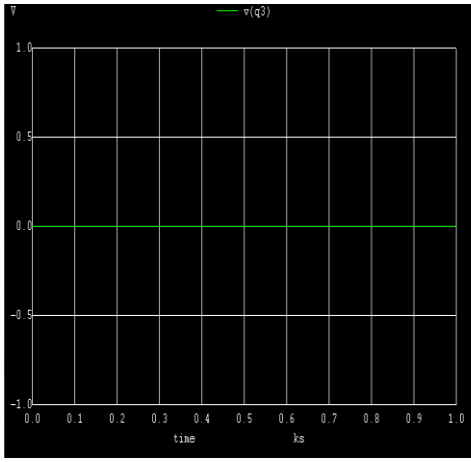

Fig13:q3 output plot

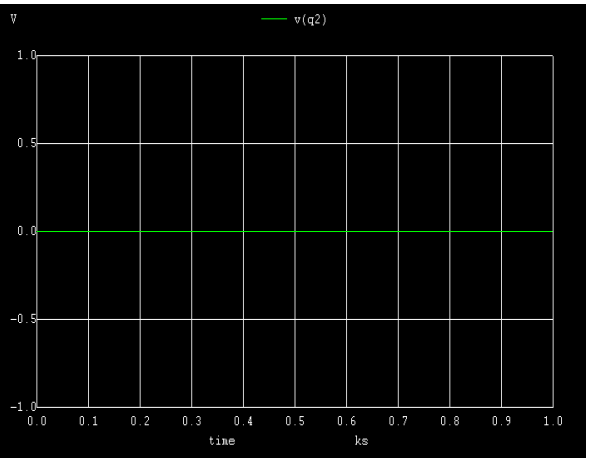

Fig14:q2 output plot

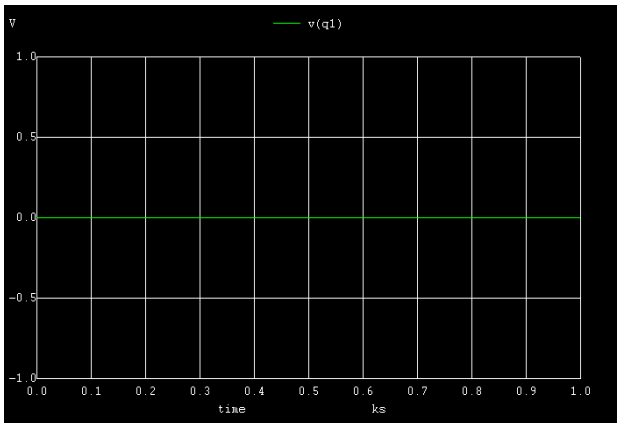

Fig15:q1 output plot

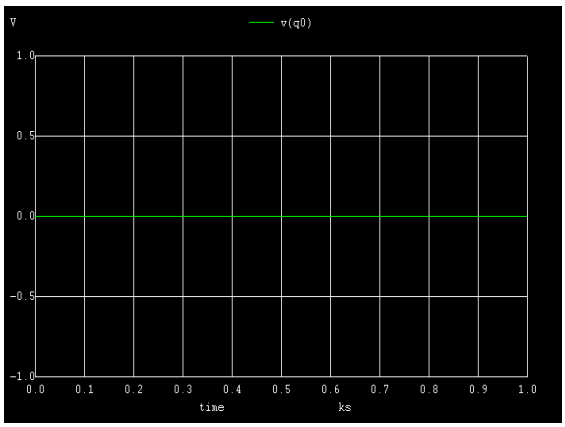

Fig16:q0 output plot

PYTHON PLOTS:

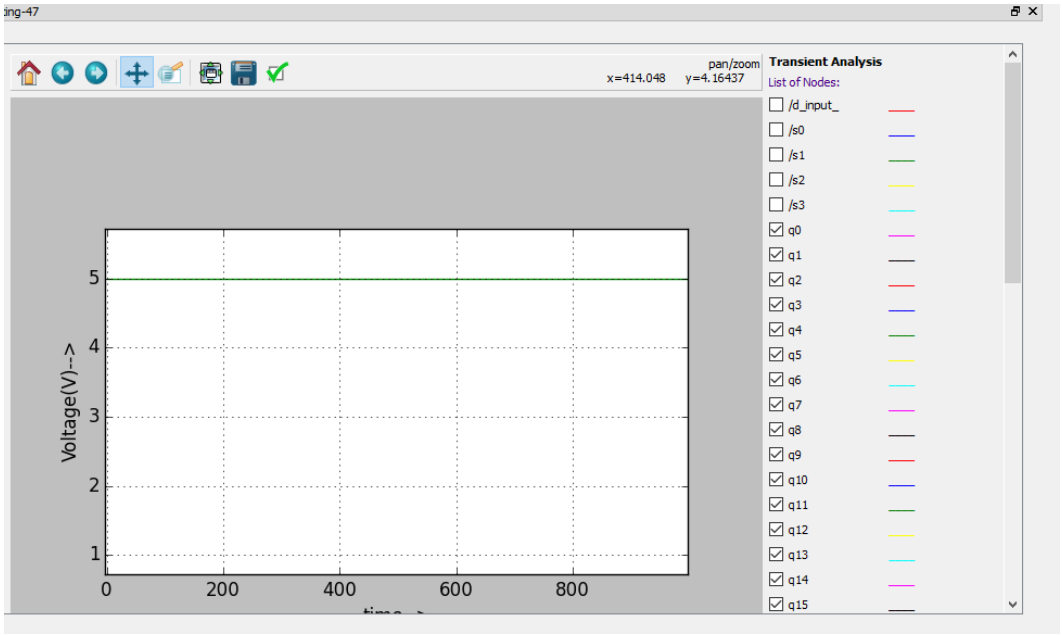

Fig:q11 output plot

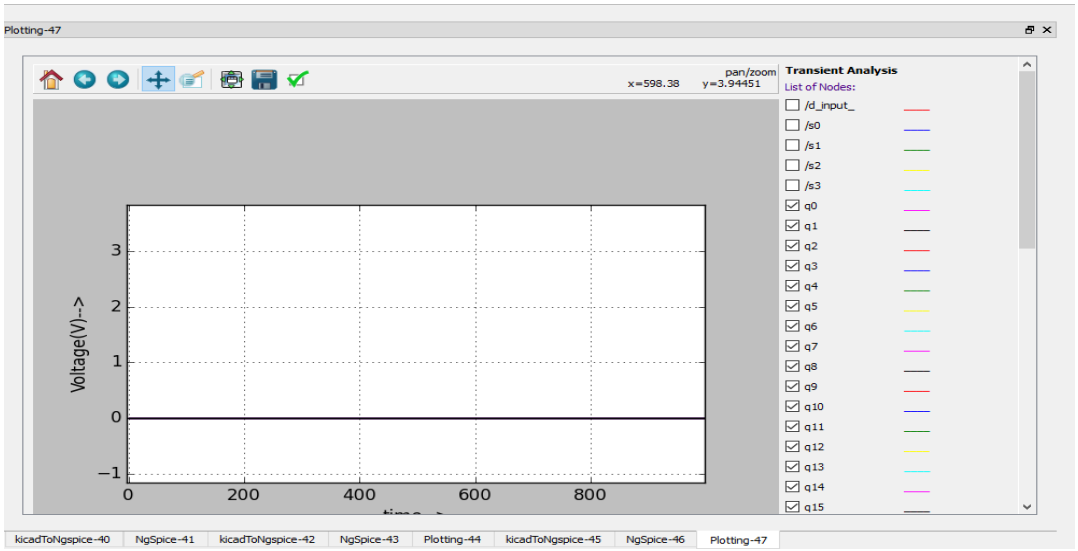

Fig:All other ooutput plots

References:

https://linus5.blogspot.in/2016/02/decoders.html

https://www.tutorialspoint.com/digital_circuits/digital_circuits_demultiplexers.htm