Scilab Textbook Companion for Op-Amps and Linear Integrated Circuit by S. Sharma[1]

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Book Description

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Scilab numbering policy used in this document and the relation to the above book.

Exa Example (Solved example)

Eqn Equation (Particular equation of the above book)

AP Appendix to Example(Scilab Code that is an Appednix to a particular Example of the above book)

For example, Exa 3.51 means solved example 3.51 of this book. Sec 2.3 means a scilab code whose theory is explained in Section 2.3 of the book.

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Chapter 1

Differential amplifiers

Scilab code Exa 1.1 Vout and CMMR

```
1  // chapter 1
2  //example 1.3
3  // page no.18,figure no.1.22
4  //given
5  Rin1=100;Rin2=100;
6  Re=2700;Rc=4700;
7  Hfe=100;
8  Hie=1000;Hoe=0;
9  Aid=(Hfe*Rc)/(Rin1+Hie);
10 disp(Aid)//differential gain
11 //Acm=(2*Re*Hoe-Hfe)*Rc/(2*Re(1+Hfe)+(Rin1+Hie)(1+2*
       Re*Hoe)),and Hoe=0
12 x=2*Re*1+2*Re*Hfe+Rin1+Hie;
13 Acm=-(Hfe*Rc)/x;
14 disp(Acm)//neglecting the negative value.taking mod
       of Acm
15 Acm=-(Acm)
16 CMRR=20*log10(Aid/Acm);
17 disp(CMRR)//is in db
18 Rin=2*Rin1+2*Hie;
19 disp(Rin)//input resistance
```

```
20 Ro=Rc
21 disp(Ro)//output resistance
```

Scilab code Exa 1.2 Icq and Vceq

```
1 // chapter 1
2 // example 1.2
3 //page 17. figure 1.21
4 //given
5 Rc=4700,Re=2700;// Resistor is in ohm
6 Vcc=12;Vee=12;// voltage is in volt
7 Vbe=.7;// assuming Vbe
8 Ie=(Vee-Vbe)/(2*Re);
9 disp(Ie)//current is in ampere
10 Icq=Ie;
11 disp(Icq)//current is in ampere
12 Vc=Icq*Rc;
13 Vce=Vcc+Vbe-Vc;
14 disp(Vce)
```

Scilab code Exa 1.3 Aid and Acm and CMRR and Ri and Ro

```
1 // chapter 1
2 // example 1.3
3 //page 18
4 Rin1=100;Rin2=100;Re=2.7*10^3;Rc=4.7*10^3;
5 hfe=100;hie=1000;hoe=0;
6 Aid=(hfe*Rc)/(Rin1+hie);//Differential gain
7 disp(Aid)
8 Acm=((2*Re*hoe-hfe)*Rc)/(2*Re*(1+hfe)+(Rin1+hie)
    *(1+2*Re*hoe));//comman mode gain
9 Acm=-Acm// neglecting negative sign
10 disp(Acm)
```

```
11 CMRR=Aid/Acm
12 CMRR=20*log10(CMRR);
13 disp(CMRR)
14 Rin=2*(Rin1+hie)//input resistance
15 Ro=Rc//output resistance
```

Scilab code Exa 1.4 constant current I

```
1 //chapter 1
2 //example 1.4
3 // page 23,figure 1.27
4 Vee=10;R1=2400;R2=2400;R3=1000;Vbe=.7;//given
5 I=(Vee-(R2*Vee/(R1+R2))-Vbe)/R3;
6 disp(I)// result is in ampere
```

Scilab code Exa 1.5 value of RE

```
1 //chapter 1
2 // example 1.5
3 //page 27.figure 1.31
4 Ic1=10*10^-6;Vcc=50;Vbe=.7;R=50*10^3;
5 Ic2=(Vcc-Vbe)/R;
6 disp(Ic2);
7 Vt=26*10^-3// assume at room temperature of 300k
8 Re=Vt/Ic1*log(Ic2/Ic1);
9 disp(Re)//result in ohm
```

Scilab code Exa 1.6 common mode op voltage and differential mode output

```
1 //chapter 3
2 // exmaple 3.6
3 //page 124 , figure 3.17
4 R1=1*10^3;R2=R1;R3=R1;//given
5 Rf=1*10^3;//given
6 Vin1=2;Vin2=1;Vin3=4;//given
7 Vout=-((Rf/R1)*Vin1+(Rf/R2)*Vin2+(Rf/R3)*Vin3);
8 disp(Vout)
```

Scilab code Exa 1.7 Dc bias point and ip and op resistance

```
1 //chapter 1
2 // example 1.7
3 //page 32,figure 1.36
4 Vee=12;Vbe=0.7;Rin=100;Re=8400;Rc=3900;Vcc=12;
5 Xdc=100// dc gain
6 Icq=(Vee-Vbe)/((Rin/Xdc)+2*Re);
7 Vceq=Vcc+Vbe-Icq*Rc;
8 disp(Vceq,Icq)//the DC base point or Q point is at(
    volt,ampere)
9 Hie=1100// assuming
10 Ri=2*(Rin+Hie);//input resistance
11 disp(Ri)// input resistance in ohm
12 Ro=Rc// output resistance
```

Scilab code Exa 1.8 Icq and Vceq voltage gain ip and op resistance

```
1 //chapter 1
2 // example 1.8
3 // page 33, figure 1.37:
4 Xdc=100;Xac=100;//AC and DC gain
5 Vbe=0.7;Vee=10;Vcc=10;// voltage is in volts
6 Re=4700;Rin=50;Rc=2700;//resistance in ohm
```

```
Hfe=100;Hie=1100// assuming
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc));
disp(Icq)//result current
Vceq=Vcc+Vbe-Rc*Icq;
disp(Vceq)// result voltage
Aid=(Hfe*Rc)/(2*(Rin+Hie));//voltage gain Aid
disp(Aid)
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//ohm
```

Scilab code Exa 1.9 operating point voltage gain ip and op resistance

```
// chapter 1
// example 1.9
//page 34, figure 1.38
Xdc=100;Xac=100;// gain
Vbe=0.7;Vee=12;Vcc=12;//given voltage in volts
Re=4700;Rin=50;Rc=2700;// given resistance in ohm
Hfe=100;Hie=1100;// given
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc));
Vceq=Vcc+Vbe-Rc*Icq;
disp(Icq,Vceq)//operating point(volt,ampere)
Aid=(Hfe*Rc)/(Rin+Hie);// voltage gain
disp(Aid)// result
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//output resistance in ohm
```

Scilab code Exa 1.10 operating point voltage gain ip and op resistance

```
// chapter 1
// example 1.10
//page 34, figure 1.39
Xdc=100;Xac=100;// gain
Vbe=0.7;Vee=12;Vcc=12;//given voltage in volts
Re=8200;Rin=150;Rc=3300;// given resistance in ohm
Hfe=100;Hie=1000;// given
Icq=(Vee-Vbe)/(2*Re+(Rin/Xdc))
Vceq=Vcc+Vbe-Rc*Icq
disp(Icq,Vceq)//operating point(volt,ampere)
Aid=(Hfe*Rc)/(Rin+Hie);// voltage gain
disp(Aid)// result
Ri=2*(Rin+Hie)// input resistance
disp(Ri)//in ohm
Ro=Rc;// output resistance
disp(Ro)//output resistance in ohm
```

Scilab code Exa 1.11 output voltage and CMRR

```
//chapter 1
// example 1.11
// page 35
Rin=1000;Rc=1000;Re=2500000;// resistance is in ohm(
    given)
Hfe=50;Hre=0;Hoe=0;Hie=1000;//given
Vid=1*10^-3;Vc=20*10^-3// voltage in volts
Aid=-(Hfe*Rc)/(Rin+Hie);// differential gain Aid
Vout=Aid*Vid;// output voltage
disp(Vout)//result in ampere.
// to calculate CMRR we have to first find Acm
    common mode gain
Acm=((2*Re*Hoe-Hfe)*Rc)/(2*Re*(1+Hfe)+Rin+Hie)//
    common mode gain
CMRR=Aid/Acm;//CMRR
disp(CMRR)//result
```

```
14 CMRRdb=20*log10(CMRR);
15 disp(CMRRdb)// result CMRR is in db
```

Scilab code Exa 1.12 DC characteristics

```
1 // chapter 1
2 // example 1.12
3 // page no.38, figure 1.44
4 Kn1=.2*10^-3;Kn2=.2*10^-3;Kn3=.4*10^-3;Kn4=.4*10^-3;
    // all in mA/V^2
5 Vtn=1;Vcc=12;Vee=-12;// voltage is in volts
6 R1=27000;Rd=15000;
7 // calculation of I1 and Vgs4
8 // applying KVL=> Vcc-Vee=I1*R1+Vgs4----------eq
    (1)
9 // I1=Kn3*(Vgs4-Vtn)^2----------eq(2)
10 // put eq (2) in eq (1)
11 //((Vcc-Vee)-Vgs4)/R1=Kn3*(Vgs4-Vtn)^2
12 p1=poly([-13.2 -20.6 10],'Vgs4','c');
13 roots(p1)// we have to take only value positive and
    greater than Vtn
14 I1=Kn3*(2.573-Vtn)^2;//only positive and value
    greater than Vtn of  Vgs4 taken
15 disp(I1)
16 //calculation  of drain current Iq
17 Iq=I1;// identical M4 and M3
18 disp(Iq)
19 // calculation of Id1 and Id2
20 Id1=Iq/2;
21 Id2=Iq/2;
22 disp(Id1,Id2)// identical
23 // calculation of gate voltage for M1 and M2
24 Vgs1=Vtn+sqrt(Id1/Kn1);// using Id1=Kn1*(Vgs1-Vtn)^2
25 disp(Vgs1)// result gate to source voltage
26 Vgs2=Vgs1;// since they are identical
```

```
27 disp(Vgs2)
28 //calculation of Vout1 and Vout2
29 Vout1=Vcc-Id1*Rd;
30 disp(Vout1)// under quiescent condition
31 Vout2=Vcc-Id2*Rd;
32 disp(Vout2)
33 // calculation of maximum common mode input voltage
     Vcmmax
34 Vds1=Vgs1-Vtn;
35 Vcmmax=Vout1-Vds1+Vgs1;//maximum common mode voltage
36 disp(Vcmmax)// result is in volts
37 // calculation of minimum common mode input voltage
     Vcmmin
38 Vds4=Vgs2-Vtn;
39 Vcmmin=Vgs1+Vds4-Vcc;// minimum common mode input
     voltage
40 disp(Vcmmin)// volts
```

Scilab code Exa 1.13 Aid Acm CMRR

```
1 // chapter 1
2 // example 1.13
3 // page 44, figure 1.52
4 Rl=%inf;B=100;Rin=0;
5 Re=1;// let suppose
6 Iq=4*10^-3;
7 Vt=26*10^-3;Va2=150;Va4=100;
8 I2=Iq/2;
9 I4=Iq/2;
10 disp(I2,I4)
11 Gm=Iq/(2*Vt);//parameters
12 Ro2=Va2/I2;
13 Ro4=Va4/I4;
14 Aid=Gm*((Ro2*Ro4)/(Ro2+Ro4));//Aid =Gm(Ro2||Ro4||Rl)
     ,Rl=%inf
```

```
15 disp(Aid)//differential mode gain Aid
16 r=(2*(B*Vt))/Iq// Vt=26mV at 300k
17 //Re=1/X*Iq and Rc=1/x*Iq/2
18 //Rc/Re=2
19 Rc=2*Re;
20 //assuming 2*(1+B)*Re/(r+Rin)>>>>1
21 //Acm=((-Gm*Rc)/1+((2*(1+B)*Re)/(r+Rin)));
22 k=(2*(1+B)*Re)/((r+Rin)/1000)
23 Acm=-((Gm*Rc)*1000)/k;
24 disp(Acm)// common mode gain
25 CMRR=Aid/-Acm;
26 disp(CMRR)//
27 CMRRdb=20*log10(CMRR);
28 disp(CMRRdb)// result is in db
```

Scilab code Exa 1.14 voltage gain and ip resistance and operating point

```
1 // chapter 1
2 //example 1.14
3 // page 46, figure1.54
4 Bac=100;Bdc=100;
5 Vbe=.715;Vd1=.715; Vz=6.2;Vee=-10;Vcc=10;Vt
     =26*10^-3;// at room temprature
6 Re=2700;Rin=10000;Rc=4700;//assuming Rin= 10k
7 Izt=41*10^-3;
8 Vin=0;// for dc analysis
9 //calculation of the value of Ie,Icq1 and Icq2
10 Vb3=Vee+Vz+Vd1
11 Ve3=Vb3-Vbe
12 Ie=(Ve3-Vee)/Re;
13 disp(Ie)
14 Ie1=Ie/2
15 Ie2=Ie/2
16 A=B/(1+B);
17 Icq=A*Ie1;//(B/(B+1))*Ie1
```

```
18 disp(Icq)
19 Icq2=Icq;
20 disp(Icq2)
21 Gm=Icq/Vt// Vt at room temp 26mA
22 r=(B*Vt)/Icq
23 Ib=Icq/B
24 Ve1=-Ib*Rin-Vbe;
25 disp(Ve1)//result
26 Vc1=Vcc-Icq*Rc;
27 disp(Vc1)
28 Vceq=Vc1-Ve1;
29 disp(Vceq,Icq)//result operating point
```

Scilab code Exa 1.15 collector current

```
1 //chapter 1
2 // example 1.15
3 //page 47, figure 1.57
4 Bdc=100;Bac=100;
5 Vbe=.715;
6 R=5600;
7 Vr=-(Vbe-10);
8 Ir=Vr/R;// Ir=Ic+Ib=Vr/R
9 disp(Ir)
10 Ic=Ir*(Bdc/(1+Bdc));//Ir=Ic+Ib=Ic+Ic/Bdc
11 disp(Ic)//ampre
12 Ic2=Ir
13 Ic3=Ir
14 Ic4=Ir
```

Scilab code Exa 1.16 smallest and largest possible value of current

```
1 //chapter 1
```

```
2 //example 1.16
3 //page 48,figure 1.59
4 Ie=400*10^-6;
5 Bmin=80;Bmax=120;
6 //Ie=Ie1+Ie2   for identical transistor Ie1=Ie2
7 Ie1=Ie/2
8 Ie2=Ie/2
9 IB1max=Ie1/(1+Bmin)
10 IB2max=Ie2/(1+Bmin)
11 IBmax=(IB1max+IB2max)/2;
12 disp(IBmax)//largest input bais current
13 IB1min=Ie1/(1+Bmax)
14 IB2min=Ie2/(1+Bmax)
15 IBmin=(IB1min+IB2min)/2;
16 disp(IBmin)// smallest current
17 Iios=IBmax-IBmin// input bais current
18 disp(Iios)//result
```

Scilab code Exa 1.17 Ri Ro differential and common mode voltage gain

```
1 //chapter1
2 //example 1.17
3 //page 49, figure 1.60
4 I=.2*10^-3; B=200;Va=100;Rl=%inf;
5 Vt=26*10^-3//assuming at room temprature
6 I2=I/2
7 I4=I2
8 r02=Va/I2;
9 disp(r02)
10 r04=Va/I4;
11 disp(r04)
12 Gm=2/Vt
13 Aid=Gm/((1/r02)+(1/r04)+(1/Rl));
14 disp(Aid)
15 Ri=2*(B/I)//Ri=2*r
```

```
16 disp(Ri)
17 Ri=(r02*r04)/(r02+r04);
18 disp(Ri)
```

Chapter 2

Operational amplifier characteristic

Scilab code Exa 2.1 value of R1

```
1 //chpter 2
2 // example 2.1
3 //page 63, figure 2.16
4 //design the value of R1 if output voltage level
     required is zero volts.
5 // given
6 Vout=0
7 Vin=6.84
8 Vbe=0.7
9 R2=270
10 //Vin-Vbe-I(R1+R2)=0 applying KVL to base emitter
11 I=(Vin-Vbe)/(R1+R2)
12 Vout=I*R2;
13 R1=1657.8-270;  // 0=(6.84-.7)270/(270+R1)
14 disp(R1) // results
```

Scilab code Exa 2.2 input bais current and input offset current

```
1 //chapter 2
2 //example 2.2
3 //page 70
4 Ib1=18*10^-6 ;Ib2=22*10^-6;// given
5 Ib=(Ib1+Ib2)/2 //input base current
6 disp(Ib) //result
7 Iios=(Ib2-Ib1) // input offset current
8 disp(Iios)// result
```

Scilab code Exa 2.3 Compensating network

```
1 //chapter 2
2 //example 2.3 page 76
3 //figure 2.36
4 Vios=8*10^-3;V=12;Vcc=12;Vee=12;//given
5 Rc=10;//let choose Rc less than 100 ohm
6 Rb=(V*Rc)/Vios //Vios=(Rc/Rb)*V
7 Rmax=Rb/10// let choose
8 Ra=Rmax*4;
9 disp(Ra)//thus resistance Ra is potentiometer which
    can be adjusted till output reaches zero value
```

Scilab code Exa 2.4 Total output offset and compensating resistance

```
1 //chapter 2
2 //example 2.4 page 79
3 //figure 2.40
4 Vios=12*10^-3; Rf=100*10^3;R1=10*10^3; Ib=500*10^-9;
    Iios=90*10^-9;//given
5 R3=Rf/R1;R4=R3+1;
6 Voos=Vios*R4+Rf*Ib;
```

```
disp(Voos)
Rcomp=R1*Rf/(R1+Rf);//Rcomp=R1||Rf
disp(Rcomp)
Voos2=Vios*R4+Rf*Iios;//with Rcomp,the output offset
    voltage become
disp(Voos2)
```

Scilab code Exa 2.5 change in output voltage

```
//chapter 2
//example 2.5 page 83
T=55-25;//chnage in temperature
A=150;//gain
Vios=.15*10^-3;//input offset voltage shift=chnage
   in output voltage/change in temp
Voos=Vios*T;//Vios=Voos/T
disp(Voos)
Vout=A*Voos;
disp(Vout)
```

Scilab code Exa 2.6 error voltage and output voltage

```
//chapter 2
//example 2.6 page83
Rf=100*10^3;R1=1*10^3//given
Viovd=14*10^-6;//input offset voltage drift
Iiocd=.5*10^-9;//input offset current drift
Vin=7*10^-3;
T=45-25;//change in tempreture
R2=Rf/R1;R3=R2+1;
Ev=R3*Viovd*T+Rf*Iiocd*T;//error voltage
disp(Ev)
A=-Rf/R1;//gain
```

```
12 Vout=A*Vin+Ev
13 Vout=A*Vin-Ev
```

Chapter 3

Basic application of Op amps

Scilab code Exa 3.1 voltage

```
1 //chpater 3
2 // example 3.1
3 //page 106, figure 3.3
4 R1=10000;Rf=47000;//given
5 Af=-(Rf/R1);// voltage gain Af=Vout/Vin
6 disp(Af)//negative sign indicate phase shift between
      input and output
```

Scilab code Exa 3.2 value of Rf

```
1 //chapter 3
2 //example 3.2
3 //page 107
4 R1=4700;
5 Af=-60;
6 Rf=Af*R1//voltage gain Af=-Rf/R1
7 disp(Rf)//result
```

Scilab code Exa 3.3 voltage gain ip and op resistance bandwidth

```
1 //chapter 3
2 // example 3.3
3 //page 112
4 A=2*10^5;//open loop gain
5 Rin=2*10^6;// input resistnace
6 Ro=75;// output resistance
7 Fo=5;// single break frequency in herzt
8 R1=470;Rf=4700;
9 K=Rf/(Rf+R1)
10 B=R1/(R1+Rf)
11 Af=-(A*Rf)/(R1+Rf+R1*A);//close loop gain
12 Rinf=R1+(Rf*Rin)/(Rf+Rin+A*Rin);
13 disp(Rinf)//close loop resistance
14 Rof=Ro/(1+A*B);//close loop output resistance
15 disp(Rof)//output resistance
16 Ff=Fo*(1+A*B);
17 disp(Ff)//bandwidth with feedback
```

Scilab code Exa 3.4 feedback resistance Rf

```
1 //chapter 3
2 // example 3.4
3 //page 114,figure 3.9
4 R1=1000;
5 Af=61;//closed loop gain
6 Rf=R1*(61-1);//Af=1+(Rf/R1)
7 disp(Rf)//feedback resistance
```

Scilab code Exa 3.5 close loop gain ip and op resistance and bandwidth

```
1 //chapter 3
2 //example 3.5
3 //page 120,
4 A=2*10^5;//open loop gain
5 R1=1000;Rf=10000;
6 Ri=2*10^6;//input resistance
7 Ro=75;//output resistance
8 Fo=5;// single break frequency in Hz
9 B=R1/(R1+Rf)
10 Af=A/(1+A*B);//gain
11 disp(Af)// closed loop gain
12 Rif=Ri*(1+A*B);// closed loop input resistance
13 disp(Rif)
14 Rof=Ro/(1+A*B);
15 disp(Rof)// colsed loop output resistance
16 Fof=Fo*(1+A*B);
17 disp(Fof)// colsed loop bandwidth in Hz
```

Scilab code Exa 3.6 output voltage

```
1 //chapter 3
2 // exmaple 3.6
3 //page 124 , figure 3.17
4 R1=1*10^3;R2=R1;R3=R1;//given
5 Rf=1*10^3;//given
6 Vin1=2;Vin2=1;Vin3=4;//given
7 Vout=-((Rf/R1)*Vin1+(Rf/R2)*Vin2+(Rf/R3)*Vin3);
8 disp(Vout)
```

Scilab code Exa 3.7 practical integrator

```
// chapter 3
// example 3.7
//page 135
A=10;//d.c gain
R1=10000;
F=10000;//input frequency
CfRf=15915*10^-4;
Fa=F/A;
Rf=10*R1;// A=Rf/R1
//Fa=1/(2*3.14*Rf*Cf)
Cf=15915*10^-4/Rf;
disp(Cf)
Rcomp=(R1*Rf)/(R1+Rf);
disp(Rcomp)
```

Scilab code Exa 3.8 maximum change in output voltage and slew rate

```
//chapter 3
//example 3.8
//page 136, figure 3.35
F=1000;
R1=1000;Cf=.1*10^-6;
Vin=5;//voltage in V
T=1/F;//time period
disp(T)// in second
Vout=(Vin*T)/(2*R1*Cf);// change in output voltage
disp(Vout)//given saturation level is 14V hence
   output will not saturate will be triangular in
   nature
S=2*%pi*F*Vin;// slew rate
disp(S)//minimum slew rate
```

Scilab code Exa 3.9 safe frequency DC gain

```
1  //chapter 3
2  //example 3.9
3  //page 137
4  R1=120*10^3;Rf=1.2*10^6;Cf=10*10^-9// given
5  fa=1/(2*%pi*Rf*Cf);// corner frequency
6  F=10*10^3;
7  Vin=5;
8  disp(fa)//coner frequency
9  safefrequency=10*fa//safe frequency is 10 times of
       corner frequency
10 Adc=Rf/R1;//D.C gain
11 Adb=20*log10(Adc)// gain in db
12 A=(Rf/R1)/sqrt(1+(F/fa)^2)//gain for practical
       intregrater circuit
13 disp(A)
14 Vout=A*Vin;//|A|=Vout(peak)/Vin(peak)
15 disp(Vout)
```

Scilab code Exa 3.11 design practical differentiator

```
1  //chapter 3
2  //example 3.11
3  //page 147
4  fa=150;fmax=150;//given
5  C1=1*10^-6;// assuming
6  Rf=1/(fa*2*%pi*C1);//fa=1/2piRfC1
7  disp(Rf)
8  fb=10*fa;// safe frequency
9  disp(fb)
10 R1=1/(2*%pi*fb*C1);//fb=1/2piC1R1
11 disp(R1)
12 Cf=((R1*C1)/Rf);//using R1C1=RfCf
13 disp(Cf)
14 Rcomp=(R1*Rf)/(R1+Rf);//rcomp=R1||Rf
15 disp(Rcomp)// generally Rcomp is selected equal to
```

R1

Scilab code Exa 3.15 scaling adder circuit

```
1 //chapter 3
2 // example 3.15
3 //page 148
4 // Vout=-(3Vin1+4Vin2+5Vin3)
5 Rf=120*10^3;
6 // for inverting summer we have Vout=-(Rf/R1Vin1+Rf/
    R2Vin2+Rf/R3Vin3)
7 R=Rf/3;//Rf/R1=3  comparing the cofficients
8 disp(R1)
9 R2=Rf/4;
10 disp(R2)
11 R3=Rf/R3;
12 disp(R3)
```

Scilab code Exa 3.16 op amp circuit

```
1 //chapter 3
2 // example 3.16
3 // page 149
4 // Vout=2Vin1-3Vin2+4Vin3-5vin4
5 Rf1=100*10^3
6 // Vout1=-(Rf1/R1Vin1+Rf1/R3Vin3)
7 R1=Rf1/2;// Rf1/R1=2  comapring the cofficient
8 R3=Rf1/4:
9 disp(R1,R2)
10 Rf2=120*10^3
11 // Vout2=-(Rf2/R2Vin1+Rf2/R4Vin3)
12 R2=Rf2/3;
13 R4=Rf2/5;
```

```
14 disp(R2,R4)
15 // output of subtracter is Vout=Vout2-Vout1
```

Scilab code Exa 3.17 find ratio of Vout by Vin

```
1  // chapter 3
2  // example 3.17
3  //page 150, figure 3.53
4  Ri=%inf;Ro=0;
5  Aol=%inf;
6  Vb=0;//b is virtually ground
7  Vout=1;// let us assume
8  //input current of op-amp is zeroas R=%inf
9  I1=(Vb-Vout)/100000
10 If2=I1;
11 Va=((10000)/(100000))*(Vb-Vout)
12 //at node A Iin=I1+If1
13 // (Vin-Va)/10*10^3=(Va-Vb)/10*10^3 + (Va-Vo)
      /100*10^3
14 Vin=Va+(10000)*((Va/10000)+((Va-Vout)/100000));
15 Ratio=Vout/Vin// result ratio of Vout/Vin
```

Scilab code Exa 3.18 output voltage in term of Vin1 and Vin2

```
1  // chapter 3
2  //example 3.18
3  // page 150, figure 3.55
4  Rf=10*10^3;R1=100*10^3;
5  Rf1=100*10^3;R11=10*10^3;
6  Vin1=1;// let suppose
7  Vin2=2
8  Vout1=(1+(Rf/R1))*Vin1;// 1st stage is non inverting
       amplifier
```

```
disp(Vout1)
// second stage there are two input Vout1 and Vin2
   aplly superposition theorem
Vout2=-(Rf1/R11)*Vout1;
//with Vout1 grounded,Vin2 active ,it behave as non-
   inverting amplifier
Vout3=(1+(Rf1/R11))*Vin2;
Vout=Vout2+Vout3;
disp(Vout)
```

Scilab code Exa 3.19 range of gain

```
// chapter 3
//example 3.19
//page 163, figure 3.73
R1=200;R2=100;Rf=100*10^3;//given
Rg1=100+0;//potentiometer resistance is 0 at start
gain1=((1+2*(Rf/Rg1))*(R2/R1));
Rg2=100+100*10^3;//potentiometer maximum value
gain2=((1+2*(Rf/Rg2))*(R2/R1));
disp(gain1,gain2)// range of gain
```

Scilab code Exa 3.20 Value of Rg

```
// chapter 3
// example 3.20
//page 164,figure 3.74
R1=100*10^3;R2=100*10^3;Rf=470;//given
// gain=(1+2Rf/Rg)(R2/R1)
gain=100;//given
Rg=(((gain/(R2/R1))-1)\(2*Rf));
disp(Rg)//result for Rg so that gain is 100
```

Scilab code Exa 3.21 transduer resistance

```
1 //chapter 3
2 //example 3.21
3 //page 167
4 Ro=100;
5 x=0.00392;
6 T1=25;//temp at 25c
7 R(25)=Ro*(1+(x*T1));
8 disp(R(25))// resistance at 25 degree
9 T2=100;
10 R(100)=Ro*(1+(x*T2));
11 disp(R(100))//resistance at 100 degree
```

Chapter 4

Non linear application of op amps

Scilab code Exa 4.1 threshold voltage

```
1 // chapter 4
2 //example 4.1
3 // page 193 ,figure 4.20
4 R1=120;R2=51*10^3;//given
5 Vsat=15;Vcc=15;Vee=15;Vin=1;//given
6 Vut=((Vsat*R1)/(R1+R2));
7 disp(Vut)//result threshold in ampere
8 Vult=((-Vsat*R1)/(R1+R2));
9 disp(Vult)//ampere
```

Scilab code Exa 4.2 Calculate value of R1 and R2

```
1 //chapter 4
2 //example 4.2
3 //page 193,figure 4.21
4 Vsat=12;Vh=6;
```

```
5 // Vh=(R1/R1+R2)(Vsat-(-Vsat))
6 R1=10000;// let assume
7 x=(Vh/(Vsat-(-Vsat)));
8 disp(x)
9 R2=((1-.25)*R1)/.25
10 disp(R2,R1)
```

Scilab code Exa 4.3 time duration

```
1 // chapter 4
2 // example 4.3
3 // page 194
4 Vp_p=5;//peak to peak volatage of sine wave
5 Vlt=-1.5;//lower threshold level
6 Vh=2;// hysteresis width
7 f=1000;
8 Vut=Vh-(-Vlt);
9 disp(Vut)
10 Vm=Vp_p/2;
11 disp(Vm)
12 //Vlt=Vm*sin(%pi+x)
13 x=36.87;// taking sin invers
14 T=1/f;
15 disp(T)
16 T1=(T*(180+x))/360;//T1 exist for angle 0 to
   (180+36.87)
17 disp(T1)
18 T2=T-T1;//t2 exist for angle 216.87 to 360
19 disp(T2)
```

Scilab code Exa 4.4 calculate Vlt Vut and Vh

```
1 // chapter 4
```

```
2 //example 4.4
3 //page 196
4 Vsat=12;
5 R1=1000;R2=3000;//given
6 Vlt=(-(+Vsat)*R1)/R2;
7 disp(Vlt)// lower threshold
8 Vut=(-(-Vsat)*R1)/R2;//upper threshold
9 disp(Vut)
10 Vh=(R1/R2)*(Vsat-(-Vsat));//hysteresis width
11 disp(Vh)
```

Scilab code Exa 4.5 change in output voltage

```
1 // chapter 4
2 // example 4.5
3 //page 220
4 Vin=5;
5 FRR=80;
6 Vout=Vin/10^4*log10(10);// FRR=20log(Vin/Vout)
7 disp(Vout);//change in output voltage
```

Chapter 6

Operational Transconductance Amplefier

Scilab code Exa 6.1 calculate frequency

```
1 //chapter 6
2 // example 6.1
3 //page 246
4 Gm=55*10^-6;
5 C=8.75*10^-12;
6 Fh=Gm/(2*3.14*C);//Fh=f-3db
7 disp(Fh)//result
```

Chapter 7

waveform generator

Scilab code Exa 7.1 calculate Vlt Vut and frequency of oscillation

```
1 //chapter 7
2 //example 7.1
3 //page 259
4 R1=86*10^3;R2=100*10^3;
5 Vsat=15;Rf=100*10^3;
6 C=.1*10^-6;
7 Vut=(R1*Vsat)/(R1+R2);
8 disp(Vut)// upper threshold
9 Vlt=(R1*(-Vsat))/(R1+R2);
10 disp(Vlt)//lower threshold
11 fo=1/(2*Rf*C)*log((Vsat-Vlt)/(Vsat-Vut));
12 disp(fo)
```

Scilab code Exa 7.2 T equal to 2RfC

```
1 //chapter7
2 // example 7.2
3 //page 259
```

```
4  R2=%s
5  R1=.86*R2
6  Vsat=%s
7  Rf=%s;
8  C=%s;
9  y=(Vsat-(R1*(-Vsat))/(R1+R2))/(Vsat-(R1*Vsat)/(R1+R2
       ))
10 g=2.72;//g=y=5.0592/1.86
11 T=2*Rf*C*log(g)// Rf=C=%s
12 disp(T)// %s*%s=s same as 2*Rf*C=2s
```

Scilab code Exa 7.3 frequency of oscillation

```
1  // chapter 7
2  // example 7.3
3  // page 276
4  R3=6000;R4=2000;//given
5  R=5100;
6  C=.001*10^-6;
7  A=1+(R3/R4);
8  if A>3 then
9    f=1/(2*3.14*R*C)
10    disp(f)//frequency of oscillation
11  end
```

Scilab code Exa 7.4 wien bridge oscillator

```
1  //chapter 7
2  //example 7.4
3  //page 277
4  C=.05*10^-6;// let choose capacitor C<1uf
5  C1=C;C2=C;
6  f=1000;
```

```
7 R=1/(2*3.14*f*C);
8 disp(R)
9 //for proper operation gain of non inverting op-amp
     must be 3
10 R4=%s
11 R3=R4*(3-1);//1+R3/R4=3
12 disp(R3)
13 R4=10000;// assume
14 R3=2*R4
15 disp(R3,R4)
```

Scilab code Exa 7.5 triangular waveform

```
1 //chapter 7
2 //example 7.5
3 // page 280
4 Vsat=15;
5 Vout=7.5;
6 fo=5000;
7 R2=10*10^3;//let assume (use a 50k POT)
8 R3=(2*Vsat*R2)/Vout;
9 disp(R3)
10 C=.01*10^-6;//let assume
11 R1=R3/(4*C*R2*fo);//fo=R3/4R1C1R2
12 disp(R1)
```

Scilab code Exa 7.6 output frequency

```
1 //chapter 7
2 //example 7.6
3 //page 285, figure 7.40
4 R1=10000;R2=5100;R3=10000;
5 C1=.001*10^-6;
```

```
V=10;
V5=(V*R3)/(R3+R2);
disp(V5)
fo=2.4*(V-V5)/(R1*C1*V);
disp(fo)
```

Scilab code Exa 7.7 monoshot using 741

```
//chapter 7
//example 7.7
// page 286,figure 7.42
R1=10000;R2=10000;
Vd1=.7;//diode drop
Vsat=12;//supply voltage
TP=2*10^-6;
C=.5*10^-9;
B=R1/(R1+R2)
//T=RCln((1+Vd1/Vsat)/(1-B))
k=((1+(Vd1/Vsat))/(1-B))
h=log(k)
R=TP/(C*h)
```

Chapter 8

Timer IC and Application

Scilab code Exa 8.1 output pulse width

```
1 // chapter 8
2 //example 8.1
3 //page 293
4 R=10*10^3;C=.1*10^-6;// given
5 t=1.1*R*C;//output pulse width
6 disp(t)//pulse widht in sec
```

Scilab code Exa 8.2 output frequency and duty cycle

```
1 //chapter 8
2 //example 8.2
3 //page 298
4 R1=4*10^3;R2=4*10^3;// given for 555 timer
5 C=.01*10^-6;//for 555 timer
6 f=1.44/((R1+2*R2)*C);
7 disp(f)//frequency of output in Hz
8 D=(R1+R2)/(R1+2*R2);
9 disp(D)//duty cycle
10 percentage=D*100
```

Scilab code Exa 8.3 timer

```
1 //chapter8
2 //example 8.3
3 //page300
4 Ton=5;//given
5 C=10*10^-6;//let assume
6 R=Ton/(1.1*C);//using Ton=1.1RC
7 disp(R)//this not standard value but we can adjust
     by connecting variable resistance
```

Scilab code Exa 8.4 design an astable multivibrator

```
1 //chapter 8
2 //example 8.4
3 //page 301
4 Toff=1;Ton=3;//given
5 C=10*10^-6;//choosing
6 R2=Toff/(.693*C);//using eq Toff=.693RC
7 disp(R2)//resistance
8 //Ton=.693(R1+R2)C
9 R1=(Ton/(.693*C))-R2;
10 disp(R1)//required resistance
```

Scilab code Exa 8.5 circuit design

```
1 //chapter8
2 //example8.5
3 //page301
```

```
T=10*10^-3;//for proper operation of LED which
   remain ON for 10msec
C=.22*10^-6//choose
Vcc=15;Vbe=.7;Vcesat=.2;//given
Vled=1.4;Iled=20*10^-3;
//T=1.1RC
R=T/(1.1*C);
disp(R)
Vo=Vcc-2*Vbe-Vcesat;//output of timer
disp(Vo)
Rled=(Vo-Vled)/Iled;
disp(Rled)//this resistance must be in series whit
   LED
f=1000;D=95;//for an astable timer
C1=.01*10^-6;
R1=%s;R2=%s;
f=1.44/(R1+2*R2)*C;//frequency----------------eq(1)
D=(R1+R2)/(R1+2*R2)//duty cycle----------------eq(2)
R2=.0555*R1;//from eq(2)
//put it in eq(1)
R1=144*10^3/(1+2*.0555);
disp(R1)
R2=.0555*R1;
disp(R2)
```

Scilab code Exa 8.6 Monostable multivibrator

```
//chapter 8
//example 8.6
//page 302
T=5*10^-3;
C=.1*10^-6;
//T=1.1RC
R=T/(1.1*C);
disp(R)//value of R should be less than 100k as
```

```
obtain above
```

Scilab code Exa 8.7 555 based square wave generater

```
1 //chapter8
2 //example8.7
3 //page 303
4 f=1000;
5 T=1/f
6 Td=T/2
7 C=.1*10^-6;
8 //Td=.69R2C
9 R2=Td/(.69*C);
10 disp(R2)
11 R1=R2//for square wave R1=R2
```

Chapter 9

Active filter

Scilab code Exa 9.1 cut off frequency

```
1 //chapter 9
2 //example 9.1
3 //page 323
4 R=10*10^3;C=.001*10^-6;
5 Rf=100*10^3;R1=10*10^3;
6 fc=1/(2*3.14*R*C);//cut off frequency
7 disp(fc)
8 Ao=1+(Rf/R1);//pass band voltage gain
9 disp(Ao)//pass band voltage gain
```

Scilab code Exa 9.2 first order low pass filter

```
1 //chapter 9
2 //example 9.2
3 //page 324
4 Ao=2;fc=10*10^3;
5 Rf=10*10^3;//let choose
6 //Ao=1+(RF/R1)
```

```
R1=Rf/(Ao-1);
disp(R1)
C=.001*10^-6;
R=1/(2*3.14*fc*C);
disp(R)
```

Scilab code Exa 9.3 second order low pass filter

```
//chapter9
//example9.3
//page327
fc=1000;
C2=.005*10^-6;R1=33*10^3;//let assume
C3=C2;C=C2;
R3=1/(2*3.14*fc*C);
disp(R3)
R2=R3
Rf=.586*R1;
disp(Rf)
```

Scilab code Exa 9.4 cutoff frequency and pass band voltage gain

```
//chapter9
//example9.4
//page327
R1=12*10^3;Rf=7*10^3;R2=33*10^3;R3=33*10^3;R
   =33*10^3;
C3=.002*10^-6;C2=.002*10^-6;C=.002*10^-6;
fc=1/2*3.14*sqrt(R2*R3*C2*C3);
disp(fc)//cut off frequency
Af=1+(Rf/R1);//passband voltage gain(Avf)
disp(Af)
```

Scilab code Exa 9.5 butterworth low pass filter

```
1 //chapter9
2 //example9.5
3 //page333
4 fc=1.5*10^3;
5 Ri=1;
6 x=sqrt(2);
7 Rf=(2-x);//for equal component model
8 disp(Rf)
9 Af=1+(Rf/Ri);//pass band gain of equal component
     model
10 Wc=2*3.14*fc;
11 C=1;
12 R=1/(Wc*C);
13 disp(R)
14 R1=R;R2=R;
15 R1=R*10^7;R2=R*10^7;//to increase R reasonable value
     we multiply R1 nad R2 by 10^7
16 disp(R1,R2)
17 C1=C*10^-7;C2=C*10^-7;//in order to keep value of fc
     unchanged we have to decrease C1 and C2 by same
     factor
18 disp(C1,C2)
```

Scilab code Exa 9.6 second order butterworth filter

```
1 //chapter 9
2 //example9.6
3 //page 335
4 fc=1.5*10^3;
5 x=1.414;//damping factor
```

```
C1=2/x;
disp(C1)
C2=x/2;
disp(C2)
R1=1;R2=1;
Rf=2;
Wc=1;
Wc=2*3.14*fc;
disp(Wc)
R=R1/Wc;//to keep C1 nad C2 unchanged
disp(R)
Rf=2*R
R1=R*10^7;R2=R*10^7;//for maiking filter for
   practical use
disp(R1,R2)
C1=C1*10^-7;C2=C2*10^-7;//to fc remain unchanged
disp(C1,C2)
```

Chapter 10

Voltage regulator

Scilab code Exa 10.1 regulated dc supply

```
1 //chapter 10
2 //example 10.1
3 //page 345
4 Vnl=12;
5 Vfl=11.6;
6 Ilmax=100*10^-3;
7 LR=Vnl-Vfl;//load regulation
8 disp(LR)
9 percentage=((Vnl-Vfl)/Vfl)*100//% LOAD REGULATION
10 Vout=LR;
11 Ro=Vout/Ilmax;//output resistance
12 disp(Ro)
```

Scilab code Exa 10.2 rms value of ripple

```
1 //chapter10
2 //example 10.2
3 //page347
```

```
4 RF=.1;//ripple factor
5 Vldc=10;
6 //ripple factor=Vrms/Vldc
7 Vrms=Vldc*RF;
8 disp(Vrms)
9 Vp_p=2*sqrt(2)*Vrms;//peak to peak ripple
10 disp(Vp_p)//volts
```

Scilab code Exa 10.3 series regulator circuit

```
1 //chapter 10
2 //example 10.3
3 //page349
4 V_=6;Vz=6;//potential at inverting(-) input is equal
      to vitual
5 Vr2=Vz;
6 Vin=30;
7 Rl=200;
8 R2=5*10^3;
9 R1=0;//for minimum Vout
10 Voutmin=((R1+R2)/R2)*Vz;//minimum output voltage
11 disp(Voutmin)//minimum voltage
12 R1=10*10^3;//for maximum output voltage
13 Voutmax=((R1+R2)/R2)*Vz;
14 disp(Voutmax)//maximum output voltage
15 disp(Voutmax,Voutmin)//range when potentiometer
     change from 0 to 10k
16 Vce=Vin-Voutmax;//when R1=10k and Vout=18
17 disp(Vce)
18 Ic=Voutmax/Rl;
19 disp(Ic)
20 Pd=Vce*Ic;//power
21 disp(Pd)//watt
```

Scilab code Exa 10.4 output voltage for regulator

```
1 //chapter 10
2 //example 10.4
3 //page 350 figure 10.9
4 Vz=5;
5 V_=5;
6 R2=15;R3=15;
7 //V_ across R3
8 Vout=((R2+R3)/R3)*(V_)//voltage across R3
9 disp(Vout)
```

Scilab code Exa 10.5 power rating

```
1 //chapter 10
2 // example 10.5
3 // page 351
4 R1=20
5 Vin=12;
6 Vout=0;//worst case  for masimum power across R1
7 VR1=Vin-Vout;
8 disp(VR1)
9 PR1=VR1^2/R1;
10 disp(PR1)//watt
```

Scilab code Exa 10.6 adjustable voltage

```
1 //chapter 10
2 //eaxmple 10.6
```

```
3 //page 354
4 Iq=4.3*10^-3;
5 R2=100;
6 Vout=7;//for maximum output voltage
7 Vr=5;//for R2 is maximum
8 //Vout=Vout(1+R2/R1)+Iq*R2
9 R1=100/(((Vout-Iq*R2)/Vr)-1)
```

Scilab code Exa 10.10 min and max output voltage for regulator

```
1 //chapter 10
2 //example 10.10
3 //page 357
4 Vref=-1.25;
5 Iadj=50*10^-6;
6 R1=240;
7 R2min=0;//to find minimum output voltage correspond
     to R2min=0
8 Voutmin=Vref*(1+(R2min/R1))+Iadj*R2min;
9 disp(Voutmin)
10 R2max=5*10^3;//for maximum output voltage
11 Voutmax=Vref*(1+(R2max/R1))+Iadj*R2max;
12 disp(Voutmax)//volts
```

Scilab code Exa 10.11 voltage IC 723

```
1 //chapter10
2 //example 10.11
3 //page 10.11
4 Vo=5;Io=50*10^-3;
5 Isc=75*10^-3;Vin=15;
6 Vsense=.6;Vref=7;
7 I=1*10^-3;//current through R1 and R2
```

```
R2=Vo/I;
disp(R2)
VR1=Vref-Vo;//voltage across R1
disp(VR1)
R1=VR1/I;
disp(R1)
R3=R1*R2/(R1+R2);//R3=R1||R2
disp(R3)
Rsc=Vsense/Isc;
disp(Rsc)
C1=7.4*10^-6/10;
disp(R1,R2,R3,Rsc,C1)//component value
```

Scilab code Exa 10.12 power dissipation in regulator

```
//chapter 10
//example 10.12
//page 372
Vref=7;Vout=5;Vin=15;
Il=1*10^-3;Isc=1.5;Vsense=.65;
Imax=150*10^-3;//Imax of IC-723 is 150mA
R1=(Vref-Vout)/Il;
disp(R1)
R2=Vout/Il;
disp(R2)
R3=(R1*R2)/(R1+R2);
disp(R3)
Rsc=Vsense/Isc;
disp(Rsc)
Bmin=Il/Imax
Pd=(Vin-Vout)*Isc
Icmax=2*Isc;//Maximum collector current
disp(Icmax)
Vout=0;//maximum collector to emitter voltage can be
    calculated as under the voltage across Q will
```

```
    maximum when the load is short circuited
Vcemax=Vin-Vout;
disp(Vcemax)
```

Scilab code Exa 10.13 design a regulated power supply

```
//chapter 10
//example 10.13
//page 373
Vref=7;Vsense=.65;
Voutmin=9;Voutmax=12; I1=.5;Imax=150*10^-3;
R2=10*10^3;//let assume
//(R1+R2)/R2=Vout/Vref----------eq(1)
R1min=2*R2/7;
disp(R1min)
Voutmax=12
R1max=5*R2/7;//using eq (1)
disp(R1max)
Rsc=Vsense/Il;
disp(Rsc)
R3=(R1max*R2)/(R1max+R2)
Bmin=Il/Imax;
disp(Bmin)
```

Scilab code Exa 10.14 current source using IC 7805

```
//chapter 10
//example 10.14
//page 376
Rl=10;Iq=4.3*10^-3;
Vr=5;Il=.5;
//  Il=Vr/R+Iq
R=Vr/(Il-Iq);
```

```
disp(R)
power=(Il^2)*R;//wattage of reisstor
disp(power)
Vout=Vr+Il*R;//output voltage with respect to ground
disp(Vout)
Vd=2;//minimum voltage drop across IC 7805 which is
   called as drop out voltage is 2V
Vin=Vout+Vd;
disp(Vin)
```

Chapter 11

Phase locked loop

Scilab code Exa 11.1 free running frequency lock range capture range

```
1 // chapter 11
2 // example 11.1
3 //page 394
4 Rt=10*10^3;Ct=.005*10^-6;C=10*10^-6;
5 V=20;//in volts
6 fout=.25/(Ct*Rt);//free running frequency
7 disp(fout)
8 fL=(8*fout)/V;//lock range
9 disp(fL)// it may be -ve or +ve
10 fc=sqrt(fL/(2*3.14*3.6*1000*C));// capture range
11 disp(fc)
```

Scilab code Exa 11.2 frequency of oscillator and phase accumulator

```
1 //chapter 11
2 //example 11.2
3 //page 401
4 foutmax=200*10^3;
```

```
5  foutmin=4;
6  n=%s;
7  fclk=2.2*foutmax;
8  disp(fclk)//maximum output frequency
9  //resolution=foutmin=fclk/2^n
10 2*n==fclk/foutmin;
11 //n=fclk/(foutmin*2);
12 //hittrail method n=17
13 n=17
14 disp(n)
```

Chapter 12

DA and AD converter

Scilab code Exa 12.1 resolution

```
1 //chapter 12
2 //example 12.1
3 // page 413
4 n=8;// number of bits
5 Vofs=2.55;//in volts
6 R=2^n;//resolution
7 disp(R)
8 Resolution=Vofs/(2^8-1);
9 disp(Resolution)// an input change of 1LSB cause the
      output to change by 10mV
```

Scilab code Exa 12.2 final output voltage

```
1 //chapter 12
2 // example 12.2
3 // page 413
4 n=4;// 4-bit DAC
5 Vofs=15;
```

```
inp=0110;
resolution=Vofs/(2^n-1);
disp(resolution)
D=0*2^3+1*2^2+1*2^1+0*2^0;//Decimal value of input
disp(D)
Vout=D*resolution
disp(Vout)
```

Scilab code Exa 12.3 Vofs and Vo

```
// chapter 12
// example 12.3
// page 414
n=8;// 8 bit DAC
R=20*10^-3;//resolution V/LSB
inpt=10000000;
Vofs=R*(2^n-1);
disp(Vofs)
D=1*2^7+0*2^6+0*2^5+0*2^4+0*2^3+0*2^2+0*2^1+0*2^0;
disp(D)
Vout=R*D;//output voltage
disp(Vout)
```

Scilab code Exa 12.4 step size and analog output

```
//chapter
//example 12.4
// page 414
n=4;// 4-bit R-2R ladder
Vofs=5;
R=Vofs/(2^n-1);//resolution
disp(R)
D1=1*2^3+0*2^2+0*2^1+0*2^0;//for input 1000
```

```
disp(D1)
Vout1=R*D1;
disp(Vout1)
D2=1*2^3+1*2^2+1*2^1+1*2^0;// for input 1111
Vout2=R*D2;
disp(Vout2)
```

Scilab code Exa 12.5 full scale output

```
//chapter 12
//example 12.5
// page 414
n=12;//12-bit DAC
R=8*10^-3;// step size
Vofs=R*(2^n-1);
disp(Vofs)
RESpercentage=(R/Vofs)*100
D
   =0*2^11+1*2^10+0*2^9+1*2^8+0*2^7+1*2^6+1*2^5+0*2^4+1*2^3+1*2^2+0*
   // decimal value of 010101101101
disp(D)
Vout=R*D;
disp(Vout)
```

Scilab code Exa 12.6 value of resistor and reference

```
//chapter 12
//example 12.6
//page 419
Vr=10;//let suppose
n=4;//4-bit R/2R ladder
Res=.5;// given Resolution
//Resolution=(1/2^n*Vr/R)*Rf
```

```
Rf=10;//let choose
R=(1/2^n)*(Vr/Res)*Rf;
disp(R)
```

Scilab code Exa 12.7 resolution and digital output

```
//chapter 12.7
// example 12.7
//page 425
n=8;//8 bit ADC
Vi=5.1;// when all output is 1
Res1=2^n;
Res2=Vi/(2^n-1);//resolution
disp(Res1,Res2)
vi=1.28;
D=vi/Res2;
disp(D)// digital output
B=(01000000)// binary equivalent of 64
```

Scilab code Exa 12.8 quantizing error

```
//chapter 12
// example 12.8
//page 426
n=12;// 12-bit ADC
Vi=4.095;//input voltage
Qe=Vi/((2^n-1)*2);// quqntizing error
disp(Qe)
```

Scilab code Exa 12.9 calculate t2

```
1 //chapter 12
2 // example 12.9
3 // page 428
4 t1=83.33;
5 Vr=100*10^-3;//reference voltage
6 Vi=100*10^-3;
7 t2=(Vi/Vr)*t1;
8 disp(t2)
9 Vi=200*10^-3;
10 t2=(Vi/Vr)*t1;
11 disp(t2)//is in msec
```

Scilab code Exa 12.10 digital output

```
1 //chapter 12
2 //example 12.10
3 //page 429
4 t1=83.33;
5 Vr=100*10^-3;// reference voltage
6 Vi=100*10^-3;//input voltage
7 Cf=12*10^3;//clock frequency
8 DIGITALVout=Cf*t1*(Vi/Vr)
9 disp(DIGITALVout)
```

Scilab code Exa 12.11 conversion time

```
1 //chapter 12
2 // example 12.11
3 //page 431
4 f=1*10^6;
5 n=8;//8-bit ADC
6 T=1/f;//time period
7 Tc=T*(n+1);
```

```
8 disp(Tc)//conversion time
```

Scilab code Exa 12.12 maximum frequency

```
1 //chapter 12
2 //example 12.12
3 //page 432
4 Tc=9*10^-6;
5 n=8;//8-bit ADC
6 fmax=1/(2*%pi*Tc*2^n);// maximum frequency
7 disp(fmax)//Hz
```