Scilab Textbook Companion for Integrated Electronics: Analog And Digital Circuits and Systems by J. Millman And C. C. Halkias[1]

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Book Description

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Scilab numbering policy used in this document and the relation to the above book.

Exa Example (Solved example)

Eqn Equation (Particular equation of the above book)

AP Appendix to Example(Scilab Code that is an Appednix to a particular Example of the above book)

For example, Exa 3.51 means solved example 3.51 of this book. Sec 2.3 means a scilab code whose theory is explained in Section 2.3 of the book.

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Chapter 1

Energy Band in Solid

Scilab code Exa 1.1 Plane Parallel plate Capacitor

```
clear;
clc;

//Caption: Plane Parallel plate Capacitor
//Given Data
d=0.001;//distance between parallel plate in m
V=1000;//applied voltage
q=1.6*(10^-19);//charge on an electron
m = 9.1*(10^-31);//mass of electron in kg
//Time taken by electron to reach other side of
   parallel plate capacitor
E=V/d;//Electric Field in V/m
//Formulae : s = u*t + (a*t^2)/2
a = (q*E)/m;//acceleration on electron in m/s^2
t = (2*d/a)^0.5;//time taken to reach the other side
    of plate
disp('sec',t,'Time taken to reach other side = ');

//Magnitude of force exerted on electron
disp('Since the potential is constant the force will
    be constant between the paltes of capacitor');
```

```
F=q*E;//force
disp('N',F,'Force on electron = ');

//Velocity of electron at the other plate
//Formulae: v = u + a*t
v = a*t;//velocity at the end of other plate
disp('m/sec',v,'v=');


//end
```

Chapter 2

Transport Phenomena in Semiconductor

Scilab code Exa 2.1.a Using Avogadro no find the numerical value of concentration of atom in Germanium

```
clear;
clc

//Example 2a
//Using Avogadro no. find the numerical value of
   concentration of atom in Germanium

//Given Values

Av=6.02*(10^23) //Avogadro No.
m=72.6 //Molar mass of germanium in gm/moles
d=5.32//density in gm/cm^3

conc = (Av/m)*d //Concentration of atom in germanium

disp('atom/cm^3',conc,'The concentration of
   germanium atom is=');

```

```
//End
```

Scilab code Exa 2.1.b Resistivity of intrinsic Germanium

```
clear;
clc

//Example 2b
//To find the resistivity of intrinsic germanium at
   300K

//Given Values

Av=6.02*(10^23) //Avogadro No.
m=72.6 //Molar mass of germanium in gm/moles
d=5.32//density in gm/cm^3
ni=2.5*(10^13);//in cm^-3
n=ni;
p=ni;//n=magnitude of free electrons , p=magnitude of
    holes , ni=magnitude of intrinsic concentration
q=1.6*(10^-19);//Charge of an Electron
yn=3800;//in cm^2/V-s
yp=1800;//in cm^2/V-s

//Required Formula
A=ni*q*(yn+yp); //Conductivity
disp('ohm-cm^-1',A,'Conductivity is =');

R =1/A //Resistivity
disp('ohm-cm',R,'Resistivity is =');

//End
```

Scilab code Exa 2.1.c Resistivity with given condition in germanium atoms

```
clear;
clc;

disp('We know that n=p=ni where n is conc of free electron p is conc of holes and ni is conc of intrinsic carriers');
//Given data
//Resistivity if 1 donor atom per 10^8 germanium atoms
Nd=4.41*(10^14);//in atoms/cm^3
ni=2.5*(10^13);//in cm^3
yn=3800;//in cm^2/V-s
q=1.6*(10^-19);

n=Nd;
p=(ni^2)/Nd;

disp('holes/cm^3',p,'the concentration of holes is=');
if(n>p)
    A=n*q*yn;//Conductivity
    disp('ohm-cm^-1',A,'The conductivity is =');
end

R=1/A;//Resistivity
disp('ohm-cm',R,'The resistivity is=');


//End
```

Scilab code Exa 2.1.d Ratio of Conductivities

```
clear;
```

```
clc;

disp('We know that n=p=ni where n is conc of free electron p is conc of holes and ni is conc of intrinsic carriers');
//Given data
//Ratio of Conductivities
Nd=4.41*(10^14);//in atoms/cm^3
ni=2.5*(10^13);//in cm^3
yn=3800;//in cm^2/V-s
q=1.6*(10^-19);

n=Nd;
A=n*q*yn;//Conductivity

//If germanium atom were monovalent metal , ratio of conductivity to that of n-type semiconductor

n=4.41*(10^22);//in electrons/cm^3

disp('If germanium atom were monovalent metal');
A1=n*q*yn;
disp('ohm-cm^-1',A1,'the coductivity of metal is=');

F=A1/A;
disp(F,'The factor by which the coductivity of metal is higher than that of n type semiconductor is');

//End
```

Chapter 5

Transistor Characteristic

Scilab code Exa 5.1.a To find transistor currents for npn transistor

```
clear;
clc;

//Example 1.1
//Caption : Program to find transistor currents for
   npn transistor.

//Given Values

//Silicon Transistor
B=100;    //Beta
Ico=20;   //in nA
Rc=3;
Rb=200;
Vbb=5;    //in V
Vcc=10; //in V
Vbe=0.7;  //in Active region

//Applying KVL to base circuit

//Vbb+Rb*Ib+Vbe=0
```

```
Ib=(Vbb-Vbe)/Rb;  //in mA

//Ico<<Ib

Ic=B*Ib;  //in mA

//To verify the Active region Assumption

//Vcc+Rc*Ic+Vcb+Vbe=0

Vcb=(-Rc*Ic)+Vcc-Vbe;  //in V

disp('V',Vcb,'Vcb = ');

if(Vcb>0)
  disp('Positive value of Vcb represents reversed
     biased collector junction and Transistor in
     active region');
end

disp('mA',Ic,'Current in transistor(Ic) is ');

disp('mA',Ib,'Current in transistor(Ib) is ');

//End
```

Scilab code Exa 5.1.b To find transistor currents for npn transistor after adding resistor to circuit

```
clear;
clc;

//Example 1.2
//Caption : Program to find transistor currents for
```

```
    npn transistor after adding resistor to circuit.

//Given Values

//Silicon Transistor
B=100;   //Beta
Ico=20;  //in nA
Rc=3;
Ico=20;  //in nA
Rb=200;
Re=2;
Vbb=5;   //in V
Vcc=10; //in V
Vbe=0.7;  //in Active region

//Ico<<Ib  Assuming

//Itot=Ib+Ic=Ib+B*Ib=(B+1)*Ib

//Applying KVL to base circuit

//Vbb+Rb*Ib+Vbe+Re*Itot=0

Ib=(Vbb-Vbe)/(Rb+(Re*(B+1)));  //in mA

Ic=B*Ib;  //in mA

//Hence Ico<<Ib

//To verify the Active region Assumption

//Vcc+Rc*Ic+Vcb+Vbe=0

Vcb=(-Rc*Ic)+Vcc-Vbe-(Re*(B+1)*Ib);  //in V

disp('V',Vcb,'Vcb = ');

if(Vcb>0)
```

```
  disp('Positive value of Vcb represents reversed
     biased collector junction and Transistor in
     active region');
end

disp('mA',Ic,'Current in transistor(Ic) is ');

disp('mA',Ib,'Current in transistor(Ib) is ');


//End
```

Scilab code Exa 5.2.a Check whether transistor is in saturation region or not

```
clear;
clc;

//Caption : Program to find transistor currents for
   npn transistor and check whether transistor is in
    saturation region or not.

//Given Values

//Silicon Transistor

Rc=3;
Rb=50;
Vbb=5;    //in V
Vcc=10; //in V
Vce=0.2; //in V
Vbe=0.8;  //in Active region
hFE=100;

//Assuming transistor in saturated region
```

```

//Applying KVL to base circuit

//Vbb+Rb*Ib+Vbe=0

Ib=(Vbb-Vbe)/Rb;   //in mA

//Applying KVL to Collector circuit

//Vcc+Rc*Ic+Vce=0

Ic=(Vcc-Vce)/Rc;   //in mA

Ib_min=Ic/hFE;

disp('mA',Ib_min,'Minimum Ib = ');

if(Ib>Ib_min)
  disp('Transistor in saturated Region');
end

disp('mA',Ic,'Current in transistor(Ic) is');

disp('mA',Ib,'Current in transistor(Ib) is');


//End
```

Scilab code Exa 5.2.b Check whether transistor is in saturation region or not after adding a Emitter Transistor

```
clear;
clc;

//Caption : Program to find transistor currents for
```

```
npn transistor and check whether transistor is in
 saturation region or not after adding a Emitter
Transistor.

//Given Values

//Silicon Transistor

Beta=100;   //Beta
Rc=3;
Rb=50;
Re=2;
Vbb=5;   //in V
Vcc=10; //in V
Vce=0.2; //in V
Vbe=0.8;  //in Active region
hFE=100;

//Assuming transistor in saturated region

//Applying KVL to base circuit

//-Vbb+Rb*Ib+Vbe+Re*(Ic+Ib)=0

//Simplifing (Rb+Re)Ib+Re*Ic=Vbb-Vbe

//Applying KVL to Collector circuit

//-Vcc+Rc*Ic+Vce+Re*(Ic+Ib)=0

//Simplifing Re*Ib+(Rc+Re)Ic=Vcc-Vce


A=[(Rb+Re) Re;Re,(Rc+Re)];
B=[(Vbb-Vbe);(Vcc-Vce)];
X=A\B;
Ib=X(1);
Ic=X(2);
```

```
Ib_min=Ic/hFE;

disp('mA',Ib_min,'Minimum Ib = ');


disp('mA',Ic,'Current in transistor(Ic)');

disp('mA',Ib,'Current in transistor(Ib)');

if(Ib>Ib_min)
  disp('Transistor in Saturated Region');
else
  disp('Transistor not in Saturated Region.Hence
     must be operating in Active region');
end

//Ico<<Ib  Assuming

//Itot=Ib+Ic=Ib+B*Ib=(B+1)*Ib

//Applying KVL to base circuit

//Vbb+Rb*Ib+Vbe+Re*Itot=0

Ib=(Vbb-Vbe)/(Rb+(Re*(Beta+1)));  //in mA

Ic=Beta*Ib;  //in mA

//Hence Ico<<Ib

//To verify the Active region Assumption

//Vcc+Rc*Ic+Vcb+Vbe=0

Vcb=(-Rc*Ic)+Vcc-Vbe-(Re*(Beta+1)*Ib);  //in V

disp('V',Vcb,'Vcb = ');
```

```
if(Vcb>0)
  disp('Positive value of Vcb represents reversed
     biased collector junction and Transistor in
     active region');
end

disp('mA',Ic,'Current in transistor(Ic) is ');

disp('mA',Ib,'Current in transistor(Ib) is ');



//End
```

Chapter 6

Digital Circuits

Scilab code Exa 6.1 Output Levels for a given input in a silicon transistor

```
clear;
clc;

//Caption:Output Levels for a given input in a silicon transistor
//Given Data
R1=15;//in K
R2=100;//in K
//R1 and R2 are voltages at base which acts as potential divider
Rc=2.2;//voltage at collector in K
hfe=30;

//For vi=0
Vb = (R1/(R1+R2))*(-12);//Voltage at base in V
disp('V',Vb,'Vb=');
//A bias of 0V is required to cut off a silicon emitter junction transistor  given in table
Vo = 0;//in V
disp('Vo',Vo,'Vo = ');

```

```
//For vi=12
vi=12;//in V
//Few standard values for silicon transistor
Vbesat=0.8;//in V
Vcesat=0.2;//in V
//Assumption: Q is in saturation region
Ic = (vi-Vcesat)/Rc;//Collector Current
disp('mA',Ic,'Ic=');
Ibmin=(Ic/hfe);//Mininmum current at the base
disp('mA',Ibmin,'Ibmin=');
I1=(vi-Vbesat)/R1;//Current in R1
I2=(Vbesat-(-12))/100;//Current in R2
Ib = I1-I2;//Base current
disp('mA',Ib,'Ib=');

if(Ib>Ibmin)
    disp('Since Ib>Ibmin , The transistor is in
       saturation region and drop is Vcesat');
    vo=Vcesat;
    disp('V',vo,'vo=');
end

//end
```

Scilab code Exa 6.2 To verify given equation

```
clear;
clc;

//Caption: To verify given equation

disp('NOTE: We will write A with a bar on its top as
      a ');
disp('To verify');
disp(' A + aB = A + B');
```

```
disp('We know that   B + 1 = 1  and  A1 = A');
disp('A + aB = A(B+1) + aB = AB + A + aB =');
disp('(A + a)B + A = B + A');
disp('which is equal to RHS')
//end
```

Scilab code Exa 6.3.a To find wether a given circuit is positive NAND

```
clear;
clc;

//Caption:To find wether a given circuit is positive
    NAND
//Given Data
R=15;//in K
R1=15;//in K
R2=100;//in K
R3=2.2;//in K
V0=0;//in V
V1=12;//in V
Vcc=12;//in V

//If input is at V0=0V
Vb = -Vcc*(R1/(R1+R2));//The base voltage of the
   transistor
disp('V',Vb,'The base voltage of transistor Vb=');
if(Vb<0)
    disp('Q is cutoff and Y is at 12V');
    disp('The result confirms the first three rows
       of truth table');
end

//If input is at V1 = 12V
//Assumption:All the diodes are reversed biased and
```

```
    transistor is in saturation
//If Q is in saturation
Vbe=0;//in V
Vp = V1*(R/(R+R1));//voltage at point P in front of
    all diodes
disp(Vp,'All diodes are reversed biased by');
Iq = (V1/(R+R1)-(V1/R2));//The base current of Q
Ic=V1/R3;//Current in the collector junction
disp('mA',Ic,'Ic=');
hFEmin = Ic/Iq;
disp(hFEmin,'hFEmin=');
disp(hFEmin,'When hFE >');
disp('Under these condition the output is at ground
    and this satisfies the first three rows of truth
    table');


//end
```

Scilab code Exa 6.3.b To find wether with given conditions NAND gate is satisfied

```
clear;
clc;

//Caption://To find wether with given conditions
    NAND gate is satisfied
//Given Data
R=15;//in K
R1=15;//in K
R2=100;//in K
R3=2.2;//in K
V0=0;//in V
V1=12;//in V
Vcc=12;//in V
```

```
//If input is at V0=0V
Vb = -Vcc*(R1/(R1+R2));//Base Current in V

//Finding thevenin equivallent fom P to ground
Rd = 1;//in K
Vd=0.7;//in v
Vr=1;//in K
//Thevenin Equivallent Voltage and resistance from P
    to ground
v = (Vcc*(Rd/(Rd+R))+(Vd*(R/(R+Rd)));
rs = Rd*(R/(R+Rd));
//Open Circuit Voltage at base of the transistor
Vb1 = (-Vcc*((R1+rs)/(R1+R2+rs)) + (v*(R2/(R1+R2+rs
    )));
disp('V',Vb1,'Vb1=');
if(Vb1>Vb)
    disp('The voltage is adequate to reverse bias Q'
        );
end


//end
```

Scilab code Exa 6.3.c Silicon Transistors and diodes are used in positive NAND

```
clear;
clc;

//Caption:Silicon Transistors and diodes are used in
    positive NAND
//Given Data
R=15;//in K
R1=15;//in K
```

```
R2=100;//in K
R3=2.2;//in K
V0=0;//in V
V1=12;//in V
Vcc=12;//in V

//To find wether with given conditions NANAD gate is
    satisfied
//Finding thevenin equivallent from P to ground
Rd = 1;//in K
Vd=0.7;//in v
Vr=1;//in K
v = (Vcc*(Rd/(Rd+R))+(Vd*(R/(R+Rd)));
rs = Rd*(R/(R+Rd));

//If the inputs are high

Vcesat = 0.2;//in V
Vb2 = (-Vcc*(R1/(R1+R2)) + ((Vd+Vcesat)*R2/(R1+R2)))
    ;
disp('V',Vb2,'Vb2=');
disp('It cuts off Q Y=1 ');

//end
```

Scilab code Exa 6.4 To verify that AND OR topology is equivallent to NAND NAND system

```
clear;
clc;

//Caption: To verify that AND-OR topology is
   equivallent to NAND-NAND system
disp('In digital electronics we have to come across
   situations where we need to use an inpout with a
```

```
   bar but here we will denote as');
disp('X with a bar = Xb and X with two bars = Xbb');

//Solution
disp('We know that X =Xbb');
disp('For AND OR logic the output of AND and
   simultaneously neglecting the input to following
   OR does not change the logic');
disp('We have also neglected the output of the OR
   gate and at the same time have added an INVERTER
   so that logic is once again unaffected');
disp('AN OR gate neglected at each terminal is an an
   AND circuit');
disp('Since AND followed by an inverter is NAND ');
disp('Hencee the NAND NAND is equivallent to AND OR'
   );

//end
```

Scilab code Exa 6.5.a To find hFEmin

```
clear;
clc;

//Caption:To find hFEmin
//Given Data
//For transistor
Vbesat=0.8;//Vgamma of diode in V
Vy=0.5;//in V
Vcesat=0.2;//in V
R = 5;//in K
Rc = 2.2;//in K

//For diode
Vyd=0.6;//in V
```

```
Vdrop=0.7;//in V

//The logic levels are Vcesato=0.2V for 0 state
Vcesato=0.2;//in V
//The logic levels are Vcc=5V for 1 state
Vcc=5;//in V
disp('If atleast one input is in 0 state');
Vp = Vcesato + Vy;//Potential at point P
disp('V',Vp,'Vp=');
//For diodes D1 and D2 to be conducting
v = 2*Vdrop;
disp('For diodes D1 and D2 to be conducting');
disp(v,'required voltage = ');
//These diodes cutoff
Vbe = 0;
if(Vbe<Vy)
    disp('Q is OFF');
    disp('Output rises to 5V and Y = 1');
    disp('This confirms first 3 rows of NAND truth table');
end

//if all inputs are at V(1)=5V , we shall assume all input diodes OFF and D1 and D2 conduct and Q is in saturation
disp('When inputs are at 5V');
Vp = Vdrop + Vdrop + Vbesat;
disp('V',Vp,'Vp=');
disp(Vcc-Vp,'The voltage across all input diode');

//For finding hFEmin
I1 = (Vcc-Vp)/R;
I2 = Vbesat/R;
Ib = I1-I2;
Ic = (Vcc-Vcesat)/Rc;
hFEmin = Ic/Ib;
disp(hFEmin,'hFEmin=');

```

```
//end
```

Scilab code Exa 6.5.b When atleast one input is at V0 in NAND gate

```
clear;
clc;

//Caption:When atleast one input is at V(0) in NAND
   gate
//Given Data
//For transistor
Vbesat=0.8;//in V
Vy=0.5;//in V
Vcesat=0.2;//in V
R = 5;//in K
Rc = 2.2;//in K

//For diode
Vyd=0.6;//Vgamma in V
Vdrop=0.7;//in V

//The logic levels are Vcesato=0.2V for 0 state
Vcesato=0.2;//in V

disp('If atleast one input is in 0 state');
Vp = Vcesato + Vdrop;//Voltage at point P
disp('V',Vp,'Vp=');
Vbe = Vp-Vyd;//Voltage at base emitter
disp('V',Vbe,'Vbe=');
if(Vbe<Vy)
    disp('Q is cutoff');
end
if(Vbe>Vy)
    disp('Q is ON');
end
```

```
//end
```

Scilab code Exa 6.5.c If input is high in NAND gate

```
clear;
clc;

//Caption:If input is high in NAND gate
//Given Data
//For transistor
Vbesat=0.8;//in V
Vy=0.5;//in V
R = 5;//in K
Rc = 2.2;//in K

//For diode
Vyd=0.6;//in V
Vdrop=0.7;//in V

//The logic levels are Vcesato=0.2V for 0 state
Vcesato=0.2;//in V

Vp = Vdrop + Vdrop + Vbesat;//Voltage at point P
disp('V',Vp,'Vp=');
disp('V',Vcc-Vp,'Each diode is reversed biased by ')
    ;
disp('V',Vyd,'A diode starts to conduct when it is
    forward bias by');
vn = (Vcc-Vp) + Vyd;//Noise Spike which will cause
    the malfunction
disp('V',vn,'A noise spike which will cause
    malfunction is');


//end
```

Scilab code Exa 6.5.d If input is low in NAND gate

```
clear;
clc;

//Caption:If input is low in NAND gate
//Given Data
//For transistor
Vbesat=0.8;//in V
Vy=0.5;//in V
R = 5;//in K
Rc = 2.2;//in K

//The logic levels are Vcesato=0.2V for 0 state
Vcesato=0.2;//in V
//For diode

Vyd=0.6;//in V
Vdrop=0.7;//in V

Vp = Vcesato + Vdrop;//Voltage at point P
disp('V',Vp,'Vp=');
Vbe = Vy;//Voltage at base emitter will be same as
    Vgamma
vp = Vbe + Vyd +Vyd;//The level to which vp should
    increase
Vn = vp - Vp;//Noise Margin
disp('V',Vn,'Noise Margin = ');

//end
```

Scilab code Exa 6.6 Calculation of FAN OUT of NAND gate

```
clear;
clc;

//Caption:Calculation of FAN OUT of NAND gate
//Given Values
hFE=30;
Vbe1active=0.7;//in V
Vd2=0.7;//in V
Vbe2sat=0.8;//in V
Vcc=5;//in V
R1=1.75;//in K
R2=2;//in K
R3=2.2;//in K
R4=5;//in K

Vp = Vbe1active + Vd2 + Vbe2sat;//Voltage at point P
//The current in 2K resistor is Ib1
//In active region
//Ic1=hFE*Ib1
//I1 = Ib1+Ic1=(1+hFE)*Ib1.... Now applying KVL between Vcc and Vp
//Vcc-Vp = R1*(1+hFE)*Ib1 + 2*Ib1
Ib1 = (Vcc-Vp)/(R1*(1+hFE)+2);//Base current in transistor 1
disp('mA',Ib1,'Ib1=');
Ic1=hFE*Ib1;//Collector Current in transistor 1
disp('mA',Ic1,'Ic1=');
I1 = Ib1 + Ic1;//in mA
I2=Vbe2sat/R4;//in mA
Ib2 = I1-I2;//Base Current in Transistor 2
//The unloaded current of Q2
Iq2=(Vcc-0.2)/R3;
//For each gate which it drive ,Q2 must sink a standard load of
I=(Vcc-Vd2-0.2)/(R1+R2);
//To Calculate the FAN OUT
//The maximum current is hFE*Ib2
//hFE*Ib2 = (I*N) + Iq2
```

```
N=((hFE*Ib2)-Iq2)/I;//FAN OUT
disp(N,'N=');

//end
```

Chapter 7

Integrated Circuit Fabrication and Characteristic

Scilab code Exa 7.1 Diffusion of a pn junction

```
clear;
clc;

//caption:Diffusion of a pn junction

disp('At distance equal to x=xi at which N =
   concentration n of doped silicon wafers , the net
    impurity density is zero. Thus xi is the
   distance at which junction  is formed');

//Given Data
q = 1.6*(10^-19);//Charge of electron
yn=1300;//mobility of silicon
p = 0.5;//resistivity in ohm-cm
y=2.2;
t=2*3600;//in sec.
xi = 2.7*(10^-4);// Junction Depth in cm.

n = 1/(p*yn*q);//Concentration of doped silicon
```

```
    wafer
disp('cm^-3',n,'The concentration  n =');
disp('The junction is formed when N = n');

//y = xi/(2*(D*t)^0.5)
D=((xi)^2/((2*y)^2*t));//Diffusion Constant

disp('cm^2/sec',D,'The value of Diffusion Constant for Boron = ');

//end
```

Scilab code Exa 7.2.a Fabrication and Characteristics

```
clear;
clc;

//Caption:Fabrication and Characteristics
//Given Data
y = 2.2;//from the figure y=2.2
Nob = 5*10^18//Uniform Concentration of Boron Profile

//y = 2.7/(2*(D*t)^0.5)
//2*(D*t)^0.5 = a
a = 2.7/y;
x = 2;//distance at which emitter junction is formed in micrometer
Nb = Nob*erfc(x/a);//boron Profile
disp('cm^-3',Nb,'Nb=');
disp('The boron diffusion equation is');
disp(a,'5*10^18*erfc x / ');
//At x=2 Np = Nb
//erfc(2/(2*(D*t)^0.5))=k
Nop=10^21;
```

```
k = Nb/Nop;
a = 2/2.7;
disp('The phosphorous diffusion equation is');
disp(a,'10^21*erfc x / ');


//end
```

Scilab code Exa 7.2.b Fabrication and Characteristics

```
clear;
clc;

//Caption:Fabrication and Characteristics
//Given Data
y = 2.2;//from the figure y=2.2
Nob = 5*10^18//Uniform Concentration of Boron
    Profile

//y = 2.7/(2*(D*t)^0.5)
//2*(D*t)^0.5 = a(let)
a = 2.7/y;
x = 2;//distance at which emitter junction is formed
     in micrometer
Nb = Nob*erfc(x/a);//boron Profile

//At x=2 Np = Nb
//erfc(2/(2*(D*t)^0.5))=k
Nop=10^21;
k = Nb/Nop;
a = 2/2.7;
//Time allowed for diffusion if diffusion of
    Phosphorous is conducted at 1100 degreeC
//From the figure D=3.8*10^-13 cm^2/sec
D=3.8*10^-13//in cm^2/sec
```

```
t = ((a*10^-4)/2)^2*(1/D);
disp('sec',t,'t=');

//end
```

Chapter 8

The Transistor at Low Frequency

Scilab code Exa 8.2 transistor as a Common Emitter Amplifier

```
clear;
clc;

//Caption:transistor as a Common Emitter Amplifier
//Given Data

Rl=10;//in K
Rs=1;//in K
hie=1.1;//in K
hre=2.5*(10^-4);
hfe=50;
hoe=25*(10^-3);//in K^-1

Ai= -hfe/(1+(hoe*Rl));//Current Gain or Current Amplification
disp(Ai,'Ai=');

Ri = hie + (hre*Rl*Ai);
disp('K',Ri,'Ri=');
```

```
Av=(Ai*Rl)/Ri;//Voltage Gain
disp(Av,'Av=');

Avs=(Av*Ri)/(Ri+Rs);//Overall Voltage Gain taking
    source resistance into account
disp(Avs,'Avs=');

Ais=(Ai*Rs)/(Ri+Rs);//Overall current gain taking
    source resistance into account
disp(Ais,'Ais=');

Yo=hoe-((hfe*hre)/(hie+Rs));//Admittance
disp('K^-1',Yo,'Yo=');

Zo = 1/Yo;//Impedence
disp('K',Zo,'Zo=');

//end
```

Scilab code Exa 8.3 To derive output impedence of given figure in open circuit voltage short circuit current theorem

```
clear;
clc;

//Caption:To derive output impedence of given figure
     in open circuit-voltage short-circuit-current
    theorem
//Solution

//Yo = I/Vo
//When current in a short circuit placed across the
    output terminals and V is the open circuit
    voltage
```

```
disp('When current in a short circuit placed across
    the output terminals and V is the open circuit
    voltage');
disp('I = -hf*I1=-(hf*Vs)/(Rs+hi)');
//Applying KVL
disp('Vs = I1*(Rs+hi)+hr*V = -ho*V*(Rs+hi)/hf+hr*V')
    ;
disp('or');
disp('V = -(hf*Vs/(Rs+hi))/(ho-hf*hr(Rs+hi))');

//end
```

Scilab code Exa 8.4 Parameters of a Common Emitter Amplifier

```
clear;
clc;

//Caption : Parameters of a Common Emitter Amplifier
//Given Data
hie=1.1;//in K
hre=2.5*(10^-4);
hfe=50;
hoe=25*(10^-3);//in K^-1
r=200;//in K
Rs=10;//in K
Ri=1;//in K
Rl=10;//in K

rl=(r*Rs)/(r+Rs);//in K

Ai = -hfe/(1+(hoe*rl));//Current Gain
disp(Ai,'Ai = ');

Ri = hie + (hre*Ai*rl);
disp('K',Ri,'Ri=');
```

```
Av=(Ai*rl)/Ri;//Voltage Gain
disp(Av,'Av = ');

k = r/(1-Av);
ri = (Ri*k)/(Ri+k);
disp('K',ri,'ri = ');

Avs = Av*(ri/(ri+Rs));//Overall voltage Gain taking
    Source resistance into account
disp(Avs,'Avs = ');

ai = Avs*((ri+Rs)/Rl);
disp(ai,'ai = -I2/I1');

//End
```

Scilab code Exa 8.5 CE CC configuration

```
clear;
 clc;

//Caption : CE-CC configuration
//Given Data
hie = 2;//in K
hfe = 50;
hre = 6*(10^-4);
hoe = 25*(10^-3);//in K^-1
hic=2;//in K
hfc=-51;
hrc=1;
hoc=25*(10^-3);///in K^-1
Re2=5;//in K
Rs=1;//in K
Rc1=5;//in K
```

```
//The Second Stage

Rl = Re2;
Ai2 = -hfc/(1+(hoc*Re2));//Current Gain in @nd
    Transistor
disp(Ai2,'Ai2=');

Ri2 = hic + (hrc*Ai2*Re2);
disp('K',Ri2,'Ri2=');

Av2 = (Ai2*Re2)/Ri2;//Voltage Gain in 2nd Transistor
disp(Av2,'Av2=');

//The First Stage

Rl1 = (Rc1*Ri2)/(Rc1+Ri2);
disp('K',Rl1,'Rl1=');

Ai1 = -hfe/(1+(hoe*Rl1));//Current Gain in 1st
    Transistor
disp(Ai1,'Ai1=');

Ri1 = hie + (hre*Ai1*Rl1);
disp('K',Ri1,'Ri1=');

Av1 = (Ai1*Rl1)/Ri1;//Voltage Gain in 1st Transistor
disp(Av1,'Av1=');

disp('The output Admittance of Transistor');
Yo1 = hoe - ((hfe*hre)/(hie+Rs));
disp('K^-1',Yo1,'Yo1=');

Ro1 = 1/Yo1;

//Output Impedence of First Stage
disp('Output Impedence of First Stage');
ro1 = (Ro1*Rc1)/(Ro1+Rc1);
```

```
disp('K',ro1,'ro1=');

rs2 = ro1;

Yo2 = hoc - ((hfc*hrc)/(hic+rs2));
disp('K^-1',Yo2,'Yo2=');

A1 = (Ai2*Ai2*Rc1)/(Ri2+Rc1);//Overall Current gain
disp(A1,'A1=');

Av = Av2*Av1;//Overall Voltage Gain
disp(Av,'Voltage Gain = Av=');

Avs = (Av*Ri1)/(Ri1+Rs);//Overall Voltage gain with Source Impedence
disp(Avs,'Overall Voltage gain taking Source Impedence into account = Avs = ');


//End
```

Scilab code Exa 8.6 Parameters of CE CC configuration

```
clear;
clc;

//Caption:Parameters of CE-CC configuration
//Given Data

hie = 2;//in K
hfe = 50;
hre = 6*(10^-4);
hoe = 25*(10^-3);//in K^-1
hic=2;//in K
hfc=-51;
```

```
hrc=1;
hoc=25*(10^-3);///in K^-1
Re2=5;//in K
Rs=5;//in K
Rc1=5;//in K

//For the CC output Stage
disp('For the CC output Stage');
Rl = Re2;
Ai2 = 1+ hfe;//Current gain in 2nd Transistor
disp(Ai2,'Ai2=');
Ri2 = hie+((1+hfe)*Rl);
disp('K',Ri2,'Ri2=');
Av2=1-(hie/Ri2);//voltage gain in 2nd transistor
disp(Av2,'Av2=');

//For the CE input Stage
disp('For the CE input Stage');

Ai1=-hfe;//Current gain in 1st transistor
Ri1 = hie;
disp(Ai1,'Ai1=');
Rl1=(Rc1*Ri2)/(Rc1+Ri2);
disp('K',Rl1,'Rl1=');
Av1=(Ai1*Rl1)/Ri1;//Voltage gain in 1st transistor
disp(Av1,'Av1=');
ro1=Rc1;
Ro2 = (hie+Rs)/(1+hfe);
ro2=(Ro2*Rl)/(Ro2+Rl);
disp('K',ro2,'Effective Source Impedence');

Av = Av1*Av2;//Overall voltage gain
disp(Av,'Overall Voltage Gain=');
Ai = Ai1*Ai2*(Rc1/(Rc1+Ri2));//Overall current Gain
disp(Ai,'Overall Current Gain=');

//End
```

Chapter 9

Transistor Biasing and Thermal Stabilization

Scilab code Exa 9.1 To find Q point

```
clear;
clc;

//Caption:To find Q point
//Given Data
Vcc=22.5//in V
Rc=5.6;//in K
Re=1;//in K
R2=10;//in K
R1=90;//in K
B=55;//beta


V=(R2*Vcc)/(R2+R1);//Thevenin Equivallent Voltage
Rb=(R2*R1)/(R2+R1);//Thevenin Equivallent Resistance
disp('Volts',V,'The equivallent Vbb =');
disp('ohm',Rb,'The equivallent Rb is');

//For base current large compared to reverse
```

```
    saturation current ie Ib>>Ico it follows that Ic=
    B*Ib

//Applying KVL to the base circuit
//0.65-2.25+Ic+10*Ib=0
disp('As B=55 we have Ic=55*Ib');

//We have   -1.60+Ic+(10/55)*Ic=0
Ic=1.60/(65/55);
Ib=Ic/55;
disp('milli amp',Ic,'Ic=');
disp('micro amp',Ib,'Ib=');

//Applying KVL to the collector circuit yields
//-22.5+6.6*Ic+Ib+Vce

Vce = 22.5-(6.6*1.36)-0.025;
disp('Volts',Vce,'Vce=');

//end
```

Scilab code Exa 9.2 To find resistances in 2N335 transistor

```
clear;
clc;

//Caption:To find resistances in 2N335 transistor
//Given Data
Rc=4;//in K
Vcc=20;//in V
Vce=10;//in V
Ic=2;//in mA
//Ic varies from 1.75 to 2.25 and B(beta) varies
    from 36 to 90

```

```
Re = (Vcc-Vce)/Ic - Rc;

//S=delta Ic/delta B
Ic2=2.25;//in mA
Ic1=1.75;//in mA
B2=90;
B1=36;
S=(Ic2-Ic1)/(B2-B1);
S2=(S*36*(1+90))/1.75;
disp(S2,'S2=','K',Re,'Re=','B2=90');

//S2=(1+B)*(1+(Rb/Re))/(1+B+(Rb/Re))
Rb=(S2-1)*(1+B2)*Re/(1+B2-S2);
disp('K',Rb,'Rb=');

Vbe=0.65;//in V
disp('V',Vbe,'We know that Vbe = ');

V = Vbe + ((Rb+Re*(1+B1))*Ic1/B1);
disp('Volts',V,'V = ');

R1=Rb*Vcc/V;
R2=R1*V/(Vcc-V);
disp('K',R1,'R1=');
disp('K',R2,'R2=');

//end
```

Scilab code Exa 9.3.a Variation of Ic in given Transistor

```
clear;
clc;

//Caption:Variation of Ic in given Transistor
//Given Data at 25degree C
```

```
Re=4.7;//in K
Rb=7.75;//in K
B1=55;//beta at 25degree C
Ic1=1.5;//in mA
Ico1=1;
Vbe1=0.6;//in V

//Part a

Ico2=33000;//in nA
Vbe2=0.225;//in V
M1=1/(1+(Rb/(Re*B1)));//Stability Factor
disp(M1,'Stabitity Factor at 25deree C=');
B2=100;//at 175degree C
M2=1/(1+(Rb/(Re*B2)));//Stability Factor
disp(M2,'Stabitity Factor at 175degree C=');

if(M2>M1)
    M1=1;
    M2=1;
end

//Let k = (delta Ic)/(Ic1)
k=(1+(Rb/Re))*(M1*(Ico2-Ico1)*(10^-9)/Ic1*(10^-3))-(M1*(Vbe2-Vbe1)/(Ic1*Re))+(1+(Rb/Re))*(M2*(B2-B1)/(B2*B1));
deltaIc=k*Ic1;
disp('mA',deltaIc,'Change in Collector Current at 175degree C is =');

//Given Data at -65degree C
 Ico2=1.95*(10^-3);
 B2=25;
 Vbe2=0.78;

 M2=1/(1+(Rb/(Re*B2)));//Stability Factor
 disp(M2,'Stabitity Factor at -65degree C=');

```

```
//Let k = (delta Ic)/(Ic1)
k=(1+(Rb/Re))*(M1*(Ico2-Ico1)*(10^-9)/Ic1*(10^-3))-(
    M1*(Vbe2-Vbe1)/(Ic1*Re))+(1+(Rb/Re))*(M2*(B2-B1)
    /(B2*B1));
deltaIc=k*Ic1;
disp('mA',deltaIc,'Change in Collector Current at
    -65degree C is =')


//End
```

Scilab code Exa 9.3.b Variation of Ic in given Transistor

```
clear;
clc;

//Caption:Variation of Ic in given Transistor
//Given Data at 25degree C
Re=4.7;//in K
Rb=7.75;//in K
B1=55;//beta at 25degree C
Ic1=1.5;//in mA
Ico1=1;
Vbe1=0.6;//in V

//Part b

Ico2=33000;//in nA
Vbe2=0.225;//in V
M1=1/(1+(Rb/(Re*B1)));//Stability Factor
//Given Data at -65degree C
 Ico2=1.95*(10^-3);
 B2=25;
 Vbe2=0.78;

```

```
 M2=1/(1+(Rb/(Re*B2)));//Stability Factor

//Let k = (delta Ic)/(Ic1)
k=(1+(Rb/Re))*(M1*(Ico2-Ico1)*(10^-9)/Ic1*(10^-3))-(M1*(Vbe2-Vbe1)/(Ic1*Re))+(1+(Rb/Re))*(M2*(B2-B1)/(B2*B1));
deltaIc=k*Ic1;


//Given Data
Ico2=32;//in nA
Vbe2=0.10;//in V
M1=1/(1+(Rb/(Re*B1)));//Stability Factor
disp(M1,'Stabitity Factor at 25deree C=');
B2=90;//at 175degree C
M2=1/(1+(Rb/(Re*B2)));//Stability Factor
disp(M2,'Stabitity Factor at 75degree C=');

if(M2>M1)
    M1=1;
    M2=1;
end

//Let k = (delta Ic)/(Ic1)
k=(1+(Rb/Re))*(M1*(Ico2-Ico1)*(10^-9)/Ic1*(10^-3))-(M1*(Vbe2-Vbe1)/(Ic1*Re))+(1+(Rb/Re))*(M2*(B2-B1)/(B2*B1));
deltaIc=k*Ic1;
disp('mA',deltaIc,'Change in Collector Current at 75 degree C is =');

//Given Data at -65degree C
 Ico2=1.95*(10^-3);
 B2=20;
 Vbe2=0.38;

 M2=1/(1+(Rb/(Re*B2)));//Stability Factor
 disp(M2,'Stabitity Factor at -65degree C=');
```

```
//Let k = (delta Ic)/(Ic1)
k=(1+(Rb/Re))*(M1*(Ico2-Ico1)*(10^-9)/Ic1*(10^-3))-(M1*(Vbe2-Vbe1)/(Ic1*Re))+(1+(Rb/Re))*(M2*(B2-B1)/(B2*B1));
deltaIc=k*Ic1;
disp('mA',deltaIc,'Change in Collector Current at -65degree C is =');

//End
```

Scilab code Exa 9.4 To design a self bias circuit

```
clear;
clc;

//Caption: To design a self bias circuit

//Given Data at 25degree C
B1=150;//beta
Ico1=50;//in nA

//Given Data at 65degree C
B2=1200;//beta
Ico2=3;//in micro A

Vbe=0.65;//in mV
Vcc=20;//in V
M=1;
//Assumption: Each factor Ico,B, and Vbe cuses the same percentge change(5%)

//Let Rb/Re=k
//(1+k)*((1200-150)/(1200*150))=0.05

```

```
k=((0.05)*((1200*150)/(1200-150)))-1;
disp(k,'Rb/Re=');
//Let us check our assumption

if(M>(1/(1+(k/B1))))
    M=1;
end

//(1+(Rb/Re))*((Ico2-Ico1)/Ic1)=0.05    Since Ico2>>
   Ico1 , we consider only Ico2

Ic1=((1+k)*Ico2)/(0.05*1000);
disp('mA',Ic1,'Ic1=');

//Vbe changes 2.5mV/degree
DVbe=2.5*40;
//Total increment
dVbe=2*DVbe*(10^-3);

//Let l=(Ic1*Re)
l=dVbe/0.05;

Re=l/Ic1;
disp(Re,'Re=');
Rb=k*Re;
disp(Rb,'Rb=');

B=(B1+B2)/2;//beta
V=((Ic1/B)*Rb)+(Vbe)+(((Ic1/B)+Ic1)*Re);
disp('Volts',V,'V=');
R1=(Rb*Vcc)/V;
R2=(R1*V)/(Vcc-V);

disp('ohm',R1,'R1=');
disp('ohm',R2,'R2=');

//end
```

Scilab code Exa 9.5 Value of theta for Ge Transistor

```
clear;
clc;

//Caption:Value of theta for Ge Transistor

//Given Data
Vcc=30;//in V
Rc=2;//in K
Re=4.7;//in K
Ic=1.5;//in mA

//We know that dPc/dIc = Vcc - (2*Ic*(Rc+Re))
//Let D=dPc/dIc

D = Vcc - (2*Ic*(Re+Rc));
disp('Ic increases by 0.131mA over a temprature range of 35 to 75 degree C');
disp('theta<(A=(dPc/dIc)*(dIc/dTc))');
A=D*((0.131*(10^-3))/(75-25));

disp('degreeC/W',1/A,'theta<');
disp('The upper bound on theta is so high that transistor would not violate it and therefore circuit will be safe from thermal runaway');

//End
```

Scilab code Exa 9.6.a To find parameters of power amplifier using pnp gemanium transistor

```
clear;
clc;

//Caption: To find parameters of power amplifier
   using pnp gemanium transistor

//Given Data
B=100;//beta
Ico=-5;//in mA
Ic=-1;//in mA
Vcc=40;
Re=5;//in ohm
Rc=10;//in ohm

//Ic= BIb + (1+B)*Ico
//Ic=B(Ib+Ico)
Ib=-(Ic/B)+Ico;
disp('mA',Ib,'Ib=');

//Neglecting Vbe
Rb=(5-Vcc)/(Ib*0.001);
disp('ohm',Rb,'Rb=');

Vce=Vcc-15;
if(Vce>(Vcc/2))
    S=(1+B)*(1+(Rb/Re))/(1+B+(Rb/Re));
    disp(S,'Stability Factor is=');
end

A=-(Vcc+(2*Ic*(Re+Rc)))*(S)*(0.007*Ico*0.01);

disp('degreeC/W',1/A,'theta=');

//end
```

Scilab code Exa 9.6.b To find parameters of power amplifier using pnp gemanium transistor

```
clear;
clc;

//Caption: To find parameters of power amplifier
   using pnp gemanium transistor

//Given Data
B=100;//beta
Ico=-5;//in mA
Ic=-1;//in mA
Vcc=40;
Re=5;//in ohm
Rc=10;//in ohm

//Ic= BIb + (1+B)*Ico
//Ic=B(Ib+Ico)
Ib=-(Ic/B)+Ico;

//Neglecting Vbe
Rb=(5-Vcc)/(Ib*0.001);

Vce=Vcc-15;
if(Vce>(Vcc/2))
    S=(1+B)*(1+(Rb/Re))/(1+B+(Rb/Re));
    disp(S,'Stability Factor is=');
end

A=-(Vcc+(2*Ic*(Re+Rc)))*(S)*(0.007*Ico*0.01);

disp('degreeC/W',1/A,'theta=');

//end
```

Chapter 10

Field Effect Transistor

Scilab code Exa 10.1.a Pinch off V and channel half width of silicon FET

```
clear;
clc;

//Caption: Pinch off V and channel half width of
   silicon FET

//Given Values
a=3*(10^-4);//in cm
Nd=10^15;//in electrons/cm^3
q=1.6*(10^-19)//in C
eo=8.85*(10^-12);//Permittivity of free space
e=12*eo;//Relative Permittivity

Vp=(q*Nd*a*a*10^6*10^-4)/(2*e);//in V
//a is in cm so 10^-4 is multiplied and Nd is in
   electrons/cm^3 so 10^6 is multiplied
disp('V',Vp,'Pinch off Voltage =');

//end
```

Scilab code Exa 10.1.b Pinch off V and channel half width of silicon FET

```
clear;
clc;

//Caption: Pinch off V and channel half width of
   silicon FET

//Given Values
a=3*(10^-4);//in m
Nd=10^15;//in electrons/m^3
q=1.6*(10^-19)//in C
eo=8.85*(10^-12);//Permittivity of free space
e=12*eo;//Relative Permittivity

Vp=(q*Nd*a*a*10^6*10^-4)/(2*e);//in V
//a is in cm so 10^-4 is multiplied and Nd is in
   electrons/cm^3 so 10^6 is multiplied
Vgs= Vp/2;

b=a*(1-((Vgs/Vp)^(0.5)));//in cm

disp('cm',b,'Channel Half Width = ');

//end
```

Scilab code Exa 10.2.a Amplifier using n channel FET

```
clear;
clc;

//Caption:amplifier using n channel FET
```

```

//Given Data

Vp=-2;//in V
Idss=1.65;//in mA
//it is desired to bias the circut at Id=0.8mA
Ids=0.8;//in mA
Vdd=24;//in V
//Assumption: rd>Rd

Vgs=Vp*(1-(Ids/Idss)^0.5);//in V
disp('V',Vgs,'Vgs=');


//end
```

Scilab code Exa 10.2.b Amplifier using n channel FET

```
clear;
clc;

//Caption:amplifier using n channel FET

//Given Data

Vp=-2;//in V
Idss=1.65;//in mA
//it is desired to bias the circut at Id=0.8mA
Ids=0.8;//in mA
Vdd=24;//in V
//Assumption: rd>Rd

Vgs=Vp*(1-(Ids/Idss)^0.5);//in V

gmo=-(2*Idss/Vp);
```

```
disp('mA/V',gmo,'gmo=');
gm=gmo*(1-(Vgs/Vp));
disp('mA/V',gm,'gm=');

//end
```

Scilab code Exa 10.2.c Amplifier using n channel FET

```
clear;
clc;

//Caption:amplifier using n channel FET

//Given Data

Vp=-2;//in V
Idss=1.65;//in mA
//it is desired to bias the circut at Id=0.8mA
Ids=0.8;//in mA
Vdd=24;//in V
//Assumption: rd>Rd

Vgs=Vp*(1-(Ids/Idss)^0.5);//in V

gmo=-(2*Idss/Vp);
gm=gmo*(1-(Vgs/Vp));

Rs=-(Vgs/Ids);//in ohm
disp('K',Rs,'Rs=');

//end
```

Scilab code Exa 10.2.d Amplifier using n channel FET

```
clear;
clc;

//Caption:amplifier using n channel FET

//Given Data

Vp=-2;//in V
Idss=1.65;//in mA
//it is desired to bias the circut at Id=0.8mA
Ids=0.8;//in mA
Vdd=24;//in V
//Assumption: rd>Rd

Vgs=Vp*(1-(Ids/Idss)^0.5);//in V

gmo=-(2*Idss/Vp);
gm=gmo*(1-(Vgs/Vp));

Rs=-(Vgs/Ids);//in ohm

disp('20dB corresponds to voltage gain of i0');
Av=10;
Rd=Av/gm;//in ohm
disp('ohm',Rd,'Rd=');

//end
```

Scilab code Exa 10.3.a To find the parameters of a FET 2N3684

```
clear;
clc;

//Caption: To find the parameters of a FET 2N3684

```

```
//Given Values
Vpmin=-2;//in V
Vpmax=-5;//in V
Idssmin=1.6;//in mA
Idssmax=7.05;//in mA
Idmin=0.8;//in mA
Ia=Idmin;
Idmax=1.2;//in mA
Ib=Idmax;
Vdd=24;//in V
Vgs1=0;//in V
Id1=0.9;//in mA
Vgs2=-4;//in V
Id2=1.1;//in mA
//Slope determines Rs
Rs=(Vgs1-Vgs2)/(Id2-Id1);
disp('ohm',Rs,'Rs=');
Vgg=Id1*Rs;
disp('V',Vgg,'Vgg=');

//end
```

Scilab code Exa 10.3.b To find the range of possible values of Id in FET 2N3684 from the graph

```
clear;
clc;

//Caption:To find the range of possible values of Id
    in FET 2N3684 from the graph

//In the figure given The line of Rs=3.3K cuts Vp =
   -2V at Id = 0.4 mA
Idmin = 0.4;//in mA
disp('mA',Idmin,'Idmin=');
```

```

//In the figure given The line of Rs=3.3K cuts Vp =
   -5V at Id = 1.2 mA
Idmax = 1.2;//in mA
disp('mA',Idmax,'Idmax=');

//end
```

Scilab code Exa 10.4 Voltage Gain of MOSFET as a single stage and then as first transistor

```
clear;
clc;

//Caption:Voltage Gain of MOSFET as a single stage
   and then as first transistor

//Given Data
Rd=100;//in K
f=20000;//frequency in Hertz
//MOSFET parameters
gm=1.6;//in mA/V
rd=44;//in k
Cgs=3*(10^-12);//in F
Cds=1*(10^-12);//in F
Cgd=2.8*(10^-12);//in F
m=gm*rd;//mew

//Required Formulae
Ygs=2*%pi*f*Cgs*%i;//in mho
Yds=2*%pi*f*Cds*%i;//in mho
Ygd=2*%pi*f*Cgd*%i;//in mho
gd=1/rd;//in mho
Yd=1/Rd;//in mho
gm=1.6*(10^-3);//in mho
```

```
disp('Gain of one stage amplifier');
Av=(-gm+Ygd)/(gd+Yd+Yds+Ygd);//Voltage Gain
disp(Av,'Av=');

disp('Gain after nelecting the interelectrode capacitance');
Av=-(m*Rd)/(Rd+rd);//Voltage Gain
disp(Av,'Av=');

//Let k= gm*Rd'
k=-Av;
Ci = (Cgs*(10^12)) +((1+k)*Cgd*(10^12));
disp('Value of Input Impedence Capacitance');
disp('pF',Ci,'Ci=');

//Now considering a two stage amplifier consisting of an FET operating
//New input Impedence taking into account various factors for present codition
Ci=200*(10^-12);
disp('Now considering a two stage amplifier consisting of an FET operating');
Yl=(0.001/Rd)+(2*%pi*f*Ci*%i);
disp(Yl,'Load Admittance =');

gd=gd*0.001;
disp('Gain');
Av=-(gm)/(gd+Yl);//Voltage Gain
disp(Av,'Av=');

//end
```

Chapter 12

MultiStage Amplifiers

Scilab code Exa 12.1.a Minimum value of coupling capacitance for a given FET

```
clear;
clc;

//Caption:Minimum value of coupling capacitance for
   a given FET
//Given Value
Ry=1;//in K
Rg=1;//in M
Ri=1;//in K
hOE=1/40;//in K^-1

//fL=1/(2*%pi*(ro+ri)*Cb)<=10
//Since ri=1M , ro<Ry=1K , then ro+ri=1M

Cb=1/(2*%pi*1*10);
disp(Cb,'Minimum Value of coupling Capacitance for
   given FET=');

//end
```

Scilab code Exa 12.1.b Minimum value of coupling capacitance for a given FET

```
clear;
clc;

//Caption:Minimum value of coupling capacitance for
   a given FET
//Given Value
Ry=1;//in K
Rg=1;//in M
Ri=1;//in K
hOE=1/40;//in K^-1

//fL=1/(2*%pi*(ro+ri)*Cb)<=10

//Ro>1/hOE=40K  ro=Rc=1K.  Rb>Ri=1K   then  ri=1K

ro=1000;//in ohm
ri=1000;//in ohm

Cb=1/(2*%pi*10*(ro+ri));
disp('pF',Cb*(10^6),'Coupling Capacitance for given
   transistor=');

//end
```

Chapter 13

Feedback Amplifier

Scilab code Exa 13.1 parameters of a Second collector to first emmitter feedback amplifier

```
clear;
clc;

//Caption : parameters of a Second collector to
   first emmitter feedback ampkifier
//Given Data
Rs=0;//in V
hfe=50;//in K
hie=1.1;//in K
hre=0;//in K
hoe=0;//in K

disp('We first calculate the effective load Rl1 at
   the first calculator');
r1=10;//in K
r2=47;//in K
r3=33;//in K
r4=1+0.1;//in K

Rl1=(r1*r2*r3*r4)/((r1*r2*r3)+(r1*r2*r4)+(r1*r3*r4)
```

```
    +(r2*r3*r4));
disp('K',Rl1,'Rl1=');

disp('Similarly for 2nd Transistor');
R1=0.1;//in K
R2=4.7;//in K
Rc1=R1+R2;
Rc2=4.7;//in K

Rl2=(Rc1*Rc2)/(Rc1+Rc2);
disp('K',Rl2,'Rl2=');

Re=(R1*R2)/(R1+R2);

disp('Voltage Gain of Transistor Q1');
Av1 = -(hfe*Rl1)/(hie+((1+hfe)*Re));
disp(Av1,'Av1=');

disp('Voltage Gain of Transistor Q2');
Av2=-(hfe*Rl2)/hie;
disp(Av2,'Av2=');

disp('Voltage Gain of two transistors in cascade
    without feedback');
Av=Av1*Av2;
disp(Av,'Av=');

B=R1/(R1+R2);//beta which is feedback
D=1+(B*Av);

Avf=Av/D;
disp(Avf,'Avf=');

disp('Input resistance without external feedback');
Ri=hie+(1+hfe)*Re;
disp('K',Ri,'Ri=');

Rif=Ri*D;
```

```
disp('K',Rif,'Rif=');

Ro=Rl2;
Rof=Ro/D;
disp('K',Rof,'Rof=');

//end
```

Scilab code Exa 13.2.a To find parameters of Current series Feedback Amplifier

```
clear;
clc;

//Caption:To find parameters of Current series
   Fwwdback Amplifier
//Given Data
Gmf=-1;//Transconductance in mA/V
D=50;//Desensivity
Avf=-4;//Voltage Gain
Rs=1;//in K
hfe=150;
Vt=0.026;//in V

Gm=Gmf*D;
disp('mA/V',Gm,'Gm=');

//B=-Re, D = 1+B*Gm = 1-B*Gm
Re=(1-D)/Gm;//in K
disp('K',Re,'Re=');

//end
```

Scilab code Exa 13.2.b To find parameters of Current series Feedback Amplifier

```
clear;
clc;

//Caption:Gain of second emitter to first
   basefeedback pair
//Given Data
Rc1=3;//in K
Rc2=0.5;//in K
Re=0.05;//in K
Rs=1.2;//in K
hfe=50;
hie=1.1;//in K
hre=0;
hoe=0;

R=Rs;

//Ai=-Ic2/Is=-(Ic2/Ib2)*(Ib2/Ic1)*(Ic1/Ib1)*(Ib1/Is)
// -Ic2/Ib2 =- hfe = -50
// Ic1/Ib1 = hfe
//Let Ib2/Ic1 = k
Ri2= hie + ((1+hfe)*(Re*R/(Re+R)));
k=-Rc1/(Rc1+Ri2);

r= Rs*(Rs+Re)/(Rs+R+Re);
//Let Ib1/Is = l
l=r/(r+hie);

Ai=(-hfe)*(k)*(hfe)*(l);

B=Re/(Re+R);//beta
D=1+(B*Ai);

Aif=Ai/D;

```

```
Avf=(Aif*Rc2)/Rs;

//To find Rif

Ri=(r*hie)/(r+hie);
Rif=Ri/D;
disp('ohm',Rif*1000,'Rif=');

//End
```

Scilab code Exa 13.2.c To find parameters of Current series Feedback Amplifier

```
clear;
clc;

//Caption:To find parameters of Current seris
   Fwwdback Amplifier
//Given Data
Gmf=-1;//Transconductance in mA/V
D=50;//Desensivity
Avf=-4;//Voltage Gain
Rs=1;//in K
hfe=150;
Vt=0.026;//in V

Gm=Gmf*D;

//B=-Re, D = 1+B*Gm = 1-B*Gm
Re=(1-D)/Gm;//in K

Rl=Avf/Gmf;//in K

// Gm= -hfe/(Rs+hie+Re)
hie= -(hfe/Gm)-Rs-Re;
```

```
Ri = Rs + hie +Re;
Rif = Ri*D
disp('K',Rif,'Rif=');


//end
```

Scilab code Exa 13.2.d To find parameters of Current seris Feedback Amplifier

```
clear;
clc;

//Caption:To find parameters of Current seris
    Feedback Amplifier
//Given Data
Gmf=-1;//Transconductance in mA/V
D=50;//Desensivity
Avf=-4;//Voltage Gain
Rs=1;//in K
hfe=150;
Vt=0.026;//in V

Gm=Gmf*D;

//B=-Re, D = 1+B*Gm = 1-B*Gm
Re=(1-D)/Gm;//in K

Rl=Avf/Gmf;//in K

// Gm= -hfe/(Rs+hie+Re)
hie= -(hfe/Gm)-Rs-Re;
Ri = Rs + hie +Re;
Rif = Ri*D

```

```
Ic=(hfe*Vt)/hie;
disp('mA',Ic,'Quiscent Collector Current = ');

//end
```

Scilab code Exa 13.3.a Gain of second emitter to first basefeedback pair

```
clear;
clc;

//Caption:Gain of second emitter to first basefeedback pair
//Given Data
Rc1=3;//in K
Rc2=0.5;//in K
Re=0.05;//in K
Rs=1.2;//in K
hfe=50;
hie=1.1;//in K
hre=0;
hoe=0;

R=Rs;

//Ai=-Ic2/Is=-(Ic2/Ib2)*(Ib2/Ic1)*(Ic1/Ib1)*(Ib1/Is)
// -Ic2/Ib2 =- hfe = -50
// Ic1/Ib1 = hfe
//Let Ib2/Ic1 = k
Ri2= hie + ((1+hfe)*(Re*R/(Re+R)));
k=-Rc1/(Rc1+Ri2);

r= Rs*(Rs+Re)/(Rs+R+Re);
//Let Ib1/Is = l
l=r/(r+hie);

```

```
Ai=(-hfe)*(k)*(hfe)*(1);
disp(Ai,'Ai=');

B=Re/(Re+R);//beta
D=1+(B*Ai);

Aif=Ai/D;
disp(Aif,'Aif=');

Avf=(Aif*Rc2)/Rs;
disp(Avf,'Avf=');

//End
```

Scilab code Exa 13.3.b Gain of second emitter to first basefeedback pair

```
clear;
clc;

//Caption:Gain of second emitter to first
    basefeedback pair
//Given Data
Rc1=3;//in K
Rc2=0.5;//in K
Re=0.05;//in K
Rs=1.2;//in K
hfe=50;
hie=1.1;//in K
hre=0;
hoe=0;

R=Rs;

//Ai=-Ic2/Is=-(Ic2/Ib2)*(Ib2/Ic1)*(Ic1/Ib1)*(Ib1/Is)
// -Ic2/Ib2 =- hfe = -50
```

```
// Ic1/Ib1 = hfe
//Let Ib2/Ic1 = k
Ri2= hie + ((1+hfe)*(Re*R/(Re+R)));
k=-Rc1/(Rc1+Ri2);

r= Rs*(Rs+Re)/(Rs+R+Re);
//Let Ib1/Is = l
l=r/(r+hie);

Ai=(-hfe)*(k)*(hfe)*(l);

B=Re/(Re+R);//beta
D=1+(B*Ai);

Aif=Ai/D;

Avf=(Aif*Rc2)/Rs;

//To find Rif

Ri=(r*hie)/(r+hie);
Rif=Ri/D;
disp('ohm',Rif*1000,'Rif=');

//End
```

Scilab code Exa 13.3.c Gain of second emitter to first basefeedback pair

```
clear;
clc;

//Caption:Gain of second emitter to first
    basefeedback pair
//Given Data
Rc1=3;//in K
```

```
Rc2=0.5;//in K
Re=0.05;//in K
Rs=1.2;//in K
hfe=50;
hie=1.1;//in K
hre=0;
hoe=0;

R=Rs;

//Ai=-Ic2/Is=-(Ic2/Ib2)*(Ib2/Ic1)*(Ic1/Ib1)*(Ib1/Is)
// -Ic2/Ib2 =- hfe = -50
// Ic1/Ib1 = hfe
//Let Ib2/Ic1 = k
Ri2= hie + ((1+hfe)*(Re*R/(Re+R)));
k=-Rc1/(Rc1+Ri2);

r= Rs*(Rs+Re)/(Rs+R+Re);
//Let Ib1/Is = l
l=r/(r+hie);

Ai=(-hfe)*(k)*(hfe)*(l);

B=Re/(Re+R);//beta
D=1+(B*Ai);

Aif=Ai/D;

Avf=(Aif*Rc2)/Rs;

Ri=(r*hie)/(r+hie);
Rif=Ri/D;

rif=(Rif*Rs)/(Rs-Rif);
disp('K',rif+Rs,'Resistance with feedback seen by
    voltage source');

//End
```

Scilab code Exa 13.3.d Gain of second emitter to first basefeedback pair

```
clear;
clc;

//Caption:Gain of second emitter to first basefeedback pair
//Given Data
Rc1=3;//in K
Rc2=0.5;//in K
Re=0.05;//in K
Rs=1.2;//in K
hfe=50;
hie=1.1;//in K
hre=0;
hoe=0;

R=Rs;

//Ai=-Ic2/Is=-(Ic2/Ib2)*(Ib2/Ic1)*(Ic1/Ib1)*(Ib1/Is)
// -Ic2/Ib2 =- hfe = -50
// Ic1/Ib1 = hfe
//Let Ib2/Ic1 = k
Ri2= hie + ((1+hfe)*(Re*R/(Re+R)));
k=-Rc1/(Rc1+Ri2);

r= Rs*(Rs+Re)/(Rs+R+Re);
//Let Ib1/Is = l
l=r/(r+hie);

Ai=(-hfe)*(k)*(hfe)*(l);

B=Re/(Re+R);//beta
D=1+(B*Ai);
```

```

Aif=Ai/D;

Avf=(Aif*Rc2)/Rs;

Rof=(Avf*Rs)/Aif;
disp('K',Rof,'Output Resistance = ');

//End
```

Scilab code Exa 13.4.a To find gain and resistance of Voltage Shunt Feedback

```
clear;
clc;

//Caption: To find gain and resistance of Voltage
   Shunt Feedback
//Given Values
Rc=4;//in K
r=40;//in K
Rs=10;//in K
hie=1.1;//in K
hfe=50;
hre=0;
hoe=0;

//Required Formulae
rc=(Rc*r)/(Rc+r);
R=(Rs*r)/(Rs+r);
Rm=-(hfe*rc*R)/(R+hie);
disp('K',Rm,'Rm=');
B=-1/r;//in mA/V
D=1+(B*Rm);
Rmf=Rm/D;
```

```
//Avf = Vo/Vs = Vo/(Is*Rs) = Rmf/Rs
Avf=Rmf/Rs;
disp(Avf,'Avf=');


//End
```

Scilab code Exa 13.4.b To find gain and resistance of Voltage Shunt Feedback

```
clear;
clc;

//Caption: To find gain and resistance of Voltage
    Shunt Feedback
//Given Values
Rc=4;//in K
r=40;//in K
Rs=10;//in K
hie=1.1;//in K
hfe=50;
hre=0;
hoe=0;

//Required Formulae
rc=(Rc*r)/(Rc+r);
R=(Rs*r)/(Rs+r);
Rm=-(hfe*rc*R)/(R+hie);
B=-1/r;//in mA/V
D=1+(B*Rm);
Rmf=Rm/D;

//Avf = Vo/Vs = Vo/(Is*Rs) = Rmf/Rs
Avf=Rmf/Rs;
```

```

Ri = (R*hie)/(R+hie);
Rif=Ri/D;
disp('K',Rif,'Rif=');

//End
```

Scilab code Exa 13.4.c To find gain and resistance of Voltage Shunt Feedback

```
clear;
clc;

//Caption: To find gain and resistance of Voltage
    Shunt Feedback
//Given Values
Rc=4;//in K
r=40;//in K
Rs=10;//in K
hie=1.1;//in K
hfe=50;
hre=0;
hoe=0;

//Required Formulae
rc=(Rc*r)/(Rc+r);
R=(Rs*r)/(Rs+r);
Rm=-(hfe*rc*R)/(R+hie);
disp('K',Rm,'Rm=');
B=-1/r;//in mA/V
D=1+(B*Rm);
Rmf=Rm/D;

//Avf = Vo/Vs = Vo/(Is*Rs) = Rmf/Rs
Avf=Rmf/Rs;
```

```

Ri = (R*hie)/(R+hie);
Rif=Ri/D;

//If the input resistance looking to the right of Rs is rif then Rif=(rif*Rs)/(rif+Rs)
rif=(Rif*Rs)/(Rs-Rif);

disp('K',Rs+rif,'The impedence seen by the voltage source=Rif=');

Ro=40;//in K
r=40;//in K

Rm = -(hfe*r*R)/(R+hie);
Rof=Ro/(1+(B*Rm));
//We are writting Rof' = rof
rof=(Rof*Rc)/(Rof+Rc);
disp('K',rof,'rof=');

//End
```

Chapter 14

Stability and Oscillators

Scilab code Exa 14.1.a Lowest poles of an Amplifier

```
clear;
clc;

//Caption:Lowest poles of an Amplifier
//Given Data

//Poles in radians per sec
s1 = -46.2*(10^5);
s2 = -45.9*(10^6);
s3 = -11.4*(10^8);
s4 = -30.4*(10^8);

//Zeros
s5 = 16.65*(10^9);
s6 = 15.4*(10^8);
s7 = -22.55*(10^8);
s = 6.28*(10^6);
B = 0.040;
Ai = 410;//Gain

n = s2/s1;
```

```
disp(n,'n=');
Q = (n*(1+(B*Ai)))^0.5/(n+1);
disp(Q,'Q=');
k = 1/(2*Q);
disp(k,'k=');

s1f = s1*((n+1)/2)*(1-%i*((4*Q*Q)-1)^0.5);
disp(s1f,'The first pole is');
s2f = s1*((n+1)/2)*(1+%i*((4*Q*Q)-1)^0.5);
disp(s2f,'The second pole is');


//end
```

Scilab code Exa 14.1.b Frequency Response Peak

```
clear;
clc;

//Frequency Response Peak
//Given Data

//Poles in radians per sec
s1 = -46.2*(10^5);
s2 = -45.9*(10^6);
s3 = -11.4*(10^8);
s4 = -30.4*(10^8);

//Zeros
s5 = 16.65*(10^9);
s6 = 15.4*(10^8);
s7 = -22.55*(10^8);
s = 6.28*(10^6);
B = 0.040;
Ai = 410;//Gain
```

```
n = s2/s1;
Q = (n*(1+(B*Ai)))^0.5/(n+1);
k = 1/(2*Q);

s1f = s1*((n+1)/2)*(1-%i*((4*Q*Q)-1)^0.5);
s2f = s1*((n+1)/2)*(1+%i*((4*Q*Q)-1)^0.5);

//Frequency Response Peak
wo = -Q*(s1+s2);
disp(wo,'wo=');
w = wo*(1-(2*k*k))^0.5//frequency at which frequency
    response peak occours
disp(w,'w=');
fpeak = (wo/s)*(1-(2*k*k))^0.5;
disp('MHz',fpeak,'fpeak=');
//At peak
a = 1/(2*k*(1-(k*k))^0.5);
overshoot = 20*log10(a);
disp('dB',overshoot,'Overshoot is');


//end
```

Chapter 15

Operational Amplifier

Scilab code Exa 15.1.a difference in output voltage for two set of output signals

```
clear;
clc;

//Caption:difference in output voltage for two set of output signals
//Given Data
//First Set of Input Signal
v11=50;//in microV
v21=-50;//in microV
//Second Set of Input Signal
v12=1050;//in microV
v22=950;//in microV
p=100;//Common Mode Rejection Ratio

//Required Formulae
//vo = Ad*vd*(1+vc/p*vd) .... p = commom mode rejection ratio
//Ad will be same for both case, So let us write Vo = vo/Ad = Ad*(1+vc/p*vd)

```

```
//First Set of Values
vd1=v11-v21;//in microV
vc1=(v11+v21)/2;//in microV
Vo1 = vd1*(1+vc1/(p*vd1));

//Second Set of Values
vd2=v12-v22;//in microV
vc2=(v12+v22)/2;//in microV
Vo2 = vd2*(1+vc2/(p*vd2));

disp(100*(Vo2-Vo1)/Vo1,'Percentage difference in
    output signal=');


//end
```

Scilab code Exa 15.1.b difference in output voltage for two set of output signals

```
clear;
clc;

//Caption:difference in output voltage for two set
    of output signals when Common Mode Rejection
    Ratio =10000
//Given Data
//First Set of Input Signal
v11=50;//in microV
v21=-50;//in microV
//Second Set of Input Signal
v12=1050;//in microV
v22=950;//in microV
p=100;//Common Mode Rejection Ratio

//Required Formulae
```

```
//vo = Ad*vd*(1+vc/p*vd) .... p = commom mode rejection ratio
//Ad  will be same for both case, So let us write Vo = vo/Ad = Ad*(1+vc/p*vd)

//First Set of Values
vd1=v11-v21;//in microV
vc1=(v11+v21)/2;//in microV
Vo1 = vd1*(1+vc1/(p*vd1));

//Second Set of Values
vd2=v12-v22;//in microV
vc2=(v12+v22)/2;//in microV
Vo2 = vd2*(1+vc2/(p*vd2));


//Now we have to calculate the same thing with common mode rejection ratio = 10000

p=10000;//Common Mode Rejection Ratio

//First Set of Values
vd1=v11-v21;//in microV
vc1=(v11+v21)/2;//in microV
Vo1 = vd1*(1+vc1/(p*vd1));

//Second Set of Values
vd2=v12-v22;//in microV
vc2=(v12+v22)/2;//in microV
Vo2 = vd2*(1+vc2/(p*vd2));

disp(100*(Vo2-Vo1)/Vo1,'Percentage difference in output signal=');

//end
```

Scilab code Exa 15.2 Design an amplifier using yA702A

```
clear;
clc;

//Caption:Design an amplifier using yA702A
//Given Data
f=32;//feedback in dB
//from the Bodes plot we get that Avo = 2510
Avo = 2510;//gain
disp('The parameters are R , r (for Rdash), C (for
    Cdash)');
//Desensivity D = B*Rmo = Avo*(R/(R+r))
//20log10(D ) = f
k = f - (20*log10(Avo));
//Let (R+r)/R = l
l = 1/(10^(k/20));
//R/(R+r) = fp/fz
//For 45degree phase margin and 32dB of low
    frequency feedback we find by trial and error
    method from the graph
fz = 10;//in MHz
fp = fz*l;
//to determine c we can arbitrarily choose R
R = 1000;//in ohm
disp('ohm',R,'R = ');
r = (l-1)*R
disp('ohm',r,'r = ');
C = 1/(2*%pi*fz*r*10^-6);
disp('pF',C,'C = ');


//end
```

Chapter 16

Integrated Circuits as Analog System Building blocks

Scilab code Exa 16.1 Fourth Order Butterworth Filter

```
clear;
clc;

//Caption:Fourth Order Butterworth Filter
//Given Data
fo=1;//Cutoff Frequency in Hz
//For n = 4
k1=0.765;
k2=1.848;

Av1 = 3-k1;
Av2 = 3-k2;
disp('For a fourth order Buttworth filter we cacade
    2 second order Buttworth filter with parameters
    R1 R2 R1d R2d R C');
//we arbitrarily choose
R1=10;//in K
disp('K',R1,'R1=');
//Av1=(R1+R1d)/R1
```

```
R1d=(Av1*R1)-R1;
disp(R1d,'R1d = ');

R2 = 10;//in K
disp('K',R2,'R2=');
R2d=(Av2*R2)-R2;
disp(R2d,'R2d = ');

//To satisfy fo = 1/(2*%pi*r*c) = 1kHz
R=1;//in K
C = 1/(2*%pi*R*fo);
disp('K',R,'R=');
disp('microF',C,'C = ');
```

Scilab code Exa 16.2 Design a second order bandpass filter

```
clear;
clc;
//Caption : Design a second order bandpass filter
//Given Value
Ao=50;//Gain
fo=160;//center frequency
B=16;//Bandwidth in Hz
C1=0.1;//in microF
C2=0.1;//in microF

//Required Formulae

Q=fo/B;
R1=(1000*Q)/(Ao*2*%pi*fo*C1);
R3=(1000*Q)/((2*%pi*fo)*(C1*C2/(C1+C2)));
//As C is in microFarad to compensate for it 1000 is
    multiplied
//Let r = R'
r=(10^6)/((2*%pi*fo)^2*R3*C1*C2);
```

```
R2=(R1*r)/(R1-r);

disp('K',R1,'R1=');
disp('K',R3,'R3=');
disp('K',r,'r=');
disp('K',R2,'R2=');

//end
```

Scilab code Exa 16.3 Design a video amplifier using MC1550

```
clear;
clc;

//Caption:Design a video amplifier using MC1550
//Given Data
Avo=-25;
Vagc=20;//in V
Vcc=6;//in V
hfe=50;
rbb=50;//in ohm
Cs=5;//in pF
Cl=5;//in pF
Ie1=1;//in mA
ft=900;//in MHz
Vt=26;//in V
n=2;//eeta
//re2 = infinity

//Since Vagc=0 , transistor Q2 is in cut off region
    and collector current of Q1 flows through Q3....
    So
Ie2=0;
Ie3=1;//in mA
re3 = (n*Vt)/Ie3;//in ohm
```

```
disp('ohm',re3,'re3=');
gm = (Ie1)/Vt;//in ohm^-1
disp('ohm^-1',gm,'gm=');
rbe=hfe/gm;
disp('ohm',rbe,'rbe=');
Ce=gm/(2*%pi*ft*10^-6);
disp('pF',Ce,'Ce=');
a3=1;//we make an assumption that alpha is one
s=0;
//Av0 = -((a3*gm)/(re3*rbb))*(1/(((1/rbb)+(1/rbe)+(s
    *Ce))*((1/re3)+(s*Cs))*((1/Rl)+(s*(Cs+Cl)))))
//From here we can find Rl
k = -((a3*gm)/(re3*rbb))*(1/(((1/rbb)+(1/rbe)+(s*Ce)
    )*((1/re3)+(s*Cs))));
Rl=Avo/k;
disp('ohm',Rl,'Rl=');

//C is in picoFarad so to compensate the whole
    equation some constants are multiplied
f1 = 1/(2*%pi*Rl*(Cs+Cl)*10^-6);
disp('MHz',f1,'f1=');
f2 = 1/(2*%pi*Ce*10^-6*((rbe*rbb)/(rbe+rbb)));
disp('MHz',f2,'f2=');
f3 = 1/(2*%pi*Cs*re3*10^-6);
disp('MHz',f3,'f3=');


//end
```

Scilab code Exa 16.4.a Logic Level Output of an ECL gate

```
clear;
clc;

//Caption:Logic Level Output of an ECL gate
```

```
//Given Data
Vbb = 1.15;//in V
Vee=5.20;//in V
Vbe5=0.7;//in V
R=1.18;//in K
r=300;//in ohm
Vbecutin=0.5;//in V

//If all inputs are low then we assume that Q1,Q2 and Q3 are cutoff and Q4 is conducting
Ve=-Vbb-Vbe5;//Voltage at Common Emitter in V
//Current I in 1.18K Resistor
I = (Ve+Vee)/R;//in mA
I1=I;
disp('mA',I,'Current in 300 ohm resistance I=');
//Output Voltage at Y
vy = -(r*I/1000)-Vbe5;//I is in mA so 1000 is multiplied
Vbe = vy-Ve;
disp('V',Vbe,'Vbe = ');
if(Vbe<Vbecutin)
    disp('Input transistors are non conducting as was assumed');
    disp('If atleast one input is high then it is assumed that curent in 1.18K resistance is switched to R and Q4 is cutoff');
    disp('Drop in 300 ohm resistance is zero.Since the base aand collector are tied together Q5 now behaves as a diode');
    disp('Across Q5');
    v=0.7;//voltage across Q5 in V
    rQ5 = 1.5;//in K
    i = (Vee-v)/rQ5;
    v = 0.75;//from the graph in V
    disp('mA',i,'i=');
    disp('V',v,'v=');
    Ve = -v-Vbe5;
    Vbe4=-Vbb-Ve;
```

```
    disp('V',Vbe4,'Vbe4=');
end
disp('The total output swing between two logic gates
    ');
vo = -vy-v;
disp('V',vo,'vo=');


//end
```

Scilab code Exa 16.4.b Calculation of noise margin

```
clear;
clc;

//Calculation of noise margin
//Given Data
Vbb = 1.15;//in V
Vee=5.20;//in V
Vbe5=0.7;//in V
R=1.18;//in K
r=300;//in ohm
Vbecutin=0.5;//in V

//If all inputs are low then we assume that Q1,Q2
    and Q3 are cutoff and Q4 is conducting
Ve=-Vbb-Vbe5;//Voltage at Common Emitter in V
//Current I in 1.18K Resistor
I = (Ve+Vee)/R;//in mA
I1=I;
//Output Voltage at Y
vy = -(r*I/1000)-Vbe5;//I is in mA so 1000 is
    multiplied
Vbe = vy-Ve;
if(Vbe<Vbecutin)
```

```
    v=0.7;//voltage across Q5 in V
    rQ5 = 1.5;//in K
    i = (Vee-v)/rQ5;
    v = 0.75;//from the graph in V
    Ve = -v-Vbe5;
    Vbe4=-Vbb-Ve;
end
vo = -vy-v;

//Calculation of noise margin
vn = Vbecutin-Vbe4;
disp('Positive noise spike which will cause the gate
    to malfunction');
disp('V',vn,'vn=');

//end
```

Scilab code Exa 16.4.c Verify that conducting transistor is in active region

```
clear;
clc;

//Verify that conducting transistor is in active
   region
//Given Data
Vbb = 1.15;//in V
Vee=5.20;//in V
Vbe5=0.7;//in V
R=1.18;//in K
r=300;//in ohm
Vbecutin=0.5;//in V

//If all inputs are low then we assume that Q1,Q2
   and Q3 are cutoff and Q4 is conducting
```

```
Ve=-Vbb-Vbe5;//Voltage at Common Emitter in V
//Current I in 1.18K Resistor
I = (Ve+Vee)/R;//in mA
I1=I;
//Output Voltage at Y
vy = -(r*I/1000)-Vbe5;//I is in mA so 1000 is multiplied
Vbe = vy-Ve;
if(Vbe<Vbecutin)
    v=0.7;//voltage across Q5 in V
    rQ5 = 1.5;//in K
    i = (Vee-v)/rQ5;
    v = 0.75;//from the graph in V
    Ve = -v-Vbe5;
    Vbe4=-Vbb-Ve;
end
vo = -vy-v;

Vb4 = Vbb;
Vc4 = -(I*r)/1000;//in V
Vcb4 = Vc4+Vb4;
disp('V',Vcb4,'Vcb4 = ');
if(Vcb4>0)
    disp('For on npn transistor this represents a reverse bias and Q4 must be in active region');
end
Vb1 = v;
Vc1 = vy+Vbe5;
Vcb1 = Vc1 + Vb1;
disp('V',Vc1,'Vc1=');
disp('V',Vcb1,'Vcb1=');
if(Vcb1<0)
    disp('For an npn transistor this represents a forward bias.... therefore Q1 is in saturation region');
    end

```

```
//end
```

Scilab code Exa 16.4.d Calculation of R

```
clear;
clc;

//Calculation of R
//Given Data
Vbb = 1.15;//in V
Vee=5.20;//in V
Vbe5=0.7;//in V
R=1.18;//in K
r=300;//in ohm
Vbecutin=0.5;//in V

//If all inputs are low then we assume that Q1,Q2
   and Q3 are cutoff and Q4 is conducting
Ve=-Vbb-Vbe5;//Voltage at Common Emitter in V
//Current I in 1.18K Resistor
I = (Ve+Vee)/R;//in mA
I1=I;
//Output Voltage at Y
vy = -(r*I/1000)-Vbe5;//I is in mA so 1000 is
   multiplied
Vbe = vy-Ve;
if(Vbe<Vbecutin)
    v=0.7;//voltage across Q5 in V
    rQ5 = 1.5;//in K
    i = (Vee-v)/rQ5;
    v = 0.75;//from the graph in V
    Ve = -v-Vbe5;
    Vbe4=-Vbb-Ve;
end
vo = -vy-v;
```

```
//Verify that conducting transistor is in active
   region
Vb4 = Vbb;
Vc4 = -(I*r)/1000;//in V
Vcb4 = Vc4+Vb4;
Vb1 = v;
Vc1 = vy+Vbe5;
Vcb1 = Vc1 + Vb1;

Vbe1 = Vbe5;
Ve = -(Vb1+Vbe1);
disp('V',Ve,'Ve=');
I = (Ve + Vee)/R;
I2=I;
R = -Vc1/I;
disp('ohm',R,'R=');

//end
```

Scilab code Exa 16.4.e Average power dissipated by the gate

```
clear;
clc;

//Average power dissipated by the gate
//Given Data
Vbb = 1.15;//in V
Vee=5.20;//in V
Vbe5=0.7;//in V
R=1.18;//in K
r=300;//in ohm
Vbecutin=0.5;//in V

//If all inputs are low then we assume that Q1,Q2
```

```
    and Q3 are cutoff and Q4 is conducting
Ve=-Vbb-Vbe5;//Voltage at Common Emitter in V
//Current I in 1.18K Resistor
I = (Ve+Vee)/R;//in mA
I1=I;
//Output Voltage at Y
vy = -(r*I/1000)-Vbe5;//I is in mA so 1000 is
    multiplied
Vbe = vy-Ve;
if(Vbe<Vbecutin)
    v=0.7;//voltage across Q5 in V
    rQ5 = 1.5;//in K
    i = (Vee-v)/rQ5;
    v = 0.75;//from the graph in V
    Ve = -v-Vbe5;
    Vbe4=-Vbb-Ve;
end

vo = -vy-v;

Vb4 = Vbb;
Vc4 = -(I*r)/1000;//in V
Vcb4 = Vc4+Vb4;
Vb1 = v;
Vc1 = vy+Vbe5;
Vcb1 = Vc1 + Vb1;

Vbe1 = Vbe5;
Ve = -(Vb1+Vbe1);
I = (Ve + Vee)/R;
I2=I;

I =(I1+I2)/2;
disp('mA',I,'I=');
I2 = (Vee-v)/rQ5;
I3 = (Vee+vy)/rQ5;
I = I + I2 + I3;
P = Vee*I;
```

```
disp('mW',P,'Power dissipated = ');

//end
```

Chapter 18

Power Circuits and Systems

Scilab code Exa 18.1.a Design a series regulated power supply

```
clear;
clc;

//Caption:Design a series regulated power supply
//Given Data
Vo=25;//in V
ro=10;//in ohm

disp('select a silicon reference diode');
disp('two IN7555 diodes are provided');
Rz = 12;//in ohm
Vo=25;//output voltage in V
Vr = 7.5 + 7.5;//because two diodes are used
Iz = 20;//in mA
Ie2=10;//in mA
Ic2 = Ie2;
Icmax=30;//in mA
Vcemax=45;//in V
hFE2=220;
hfe2=200;
hie2=800;//in ohm
```

```
Id=10;//in mA
Il = 1000;//in mA
Vi = 50;//in V
dVi = 10; //change in input voltage
dIl = 1;//change in load current

//For D1 and D2 operate
Iz = Id + Id;
Rd = (Vo-Vr)/Id;
disp('K',Rd,'Rd=');

Ib2 = (1000*Ic2)/hFE2;
disp('microA',Ib2,'Ib2=');

//Since we require I1>Ib2 , we select
I1=10*(10^-3);//in A
Vbe = 0.7;//in V

V2 = Vbe + Vr;
disp('V',V2,'V2=');

R1 = (Vo-V2)/I1;
R2 = V2/I1;
disp('ohm',R1,'R1=');
disp('ohm',R2,'R2=');

//We are selecting Texas Instruments 2N1722 silicon power transistor , so following parameters are required
disp('We are selecting Texas Instruments 2N1722 silicon power transistor');
Ic1 = 1;//in A
hFE1=125;
hfe1=100;
hie1=20;

Ib1 =(1000*I1 + Il + Id)/hFE1;
disp('mA',Ib1+Ic2,'The current through resistor R3
```

```
    is');
I=Ib1 + Ic2;

R3 = (Vi - (Vbe + Vo))/I;
disp('K',R3,'The value of R3 is');

//End
```

Scilab code Exa 18.1.b Calculation of Sv

```
clear;
clc;

//Caption:Calculation of Sv
//Given Data
Vo=25;//in V
ro=10;//in ohm

Rz = 12;//in ohm
Vo=25;//output voltage in V
Vr = 7.5 + 7.5;//because two diodes are used
Iz = 20;//in mA
Ie2=10;//in mA
Ic2 = Ie2;
Icmax=30;//in mA
Vcemax=45;//in V
hFE2=220;
hfe2=200;
hie2=800;//in ohm
Id=10;//in mA
Il = 1000;//in mA
Vi = 50;//in V
dVi = 10; //change in input voltage
dIl = 1;//change in load current

```

```
//For D1 and D2 operate
Iz = Id + Id;
Rd = (Vo-Vr)/Id;

Ib2 = (1000*Ic2)/hFE2;

//Since we require I1>Ib2 , we select
I1=10*(10^-3);//in A
Vbe = 0.7;//in V

V2 = Vbe + Vr;

R1 = (Vo-V2)/I1;
R2 = V2/I1;

//We are selecting Texas Instruments 2N1722 silicon
   power transistor, so following parameters are
   required
Ic1 = 1;//in A
hFE1=125;
hfe1=100;
hie1=20;

Ib1 =(1000*I1 + Il + Id)/hFE1;
//The current through resistor R3
I=Ib1 + Ic2;

R3 = (Vi - (Vbe + Vo))/I;
Gm = hfe2*(R2/(R2+R1))*(1/((R1*R2/(R1+R2))+hie2+(1+
   hfe2)*Rz)) ;
Sv = (10^-3)/(Gm*R3);
disp(Sv,'Sv=');

//End
```

Scilab code Exa 18.1.c Find output resistance Ro

```
clear;
clc;

//Caption:Find output resistance Ro
//Given Data
Vo=25;//in V
ro=10;//in ohm
Rz = 12;//in ohm
Vo=25;//output voltage in V
Vr = 7.5 + 7.5;//because two diodes are used
Iz = 20;//in mA
Ie2=10;//in mA
Ic2 = Ie2;
Icmax=30;//in mA
Vcemax=45;//in V
hFE2=220;
hfe2=200;
hie2=800;//in ohm
Id=10;//in mA
Il = 1000;//in mA
Vi = 50;//in V
dVi = 10; //change in input voltage
dIl = 1;//change in load current

//For D1 and D2 operate
Iz = Id + Id;
Rd = (Vo-Vr)/Id;

Ib2 = (1000*Ic2)/hFE2;

//Since we require I1>Ib2 , we select
I1=10*(10^-3);//in A
Vbe = 0.7;//in V

V2 = Vbe + Vr;

```

```
R1 = (Vo-V2)/I1;
R2 = V2/I1;

//We are selecting Texas Instruments 2N1722 silicon
   power transistor , so following parameters are
   required
Ic1 = 1;//in A
hFE1=125;
hfe1=100;
hie1=20;

Ib1 =(1000*I1 + Il + Id)/hFE1;
//The current through resistor R3 is
I=Ib1 + Ic2;

R3 = (Vi - (Vbe + Vo))/I;

Gm = hfe2*(R2/(R2+R1))*(1/((R1*R2/(R1+R2))+hie2+(1+
   hfe2)*Rz)) ;
disp(Gm,'Gm=');

Ro = (ro + (((1000*R3) + hie1)/(1+hfe1)))/(1 + (Gm
   *((1000*R3) + ro)));
disp('K',Ro,'The output impedence is = ');

//End
```

Scilab code Exa 18.1.d Calculation of change in output voltage due to change in input voltage and load current

```
clear;
clc;

//Caption:Calculation of change in output voltage
   due to change in input voltage and load current
```

```
//Given Data
Vo=25;//in V
ro=10;//in ohm

Rz = 12;//in ohm
Vo=25;//output voltage in V
Vr = 7.5 + 7.5;//because two diodes are used
Iz = 20;//in mA
Ie2=10;//in mA
Ic2 = Ie2;
Icmax=30;//in mA
Vcemax=45;//in V
hFE2=220;
hfe2=200;
hie2=800;//in ohm
Id=10;//in mA
Il = 1000;//in mA
Vi = 50;//in V
dVi = 10; //change in input voltage
dIl = 1;//change in load current

//For D1 and D2 operate
Iz = Id + Id;
Rd = (Vo-Vr)/Id;

Ib2 = (1000*Ic2)/hFE2;

//Since we require I1>Ib2 , we select
I1=10*(10^-3);//in A
Vbe = 0.7;//in V

V2 = Vbe + Vr;

R1 = (Vo-V2)/I1;
R2 = V2/I1;

//We are selecting Texas Instruments 2N1722 silicon
    power transistor , so following parameters are
```

```
    required
Ic1 = 1;//in A
hFE1=125;
hfe1=100;
hie1=20;

Ib1 =(1000*I1 + Il + Id)/hFE1;
//The current through resistor R3 is
I=Ib1 + Ic2;

R3 = (Vi - (Vbe + Vo))/I;

Gm = hfe2*(R2/(R2+R1))*(1/((R1*R2/(R1+R2))+hie2+(1+
    hfe2)*Rz)) ;
Sv = (10^-3)/(Gm*R3);

Ro = (ro + (((1000*R3) + hie1)/(1+hfe1)))/(1 + (Gm
    *((1000*R3) + ro)));

dVo = (Sv*dVi)+(Ro*dIl);
disp('V',dVo,'Change in output voltage = ');

//End
```

Scilab code Exa 18.2.a SCR half wave power control circuit

```
clear;
clc;

//Caption:SCR half wave power control circuit
//Given Data
Vs=230;//in V
Rl=200;//in ohm
//Trigger is adjusted so that conduction starts
    after 60degree of start of cycle
```

```
//Instantaneous Current il = (230*2^0.5*sin(a))/200

// to find rms value
xo = %pi/3;//lower limit of integration
x1 = %pi;//upper limit of integration

X = integrate('((230*(2^0.5)*sin(x))/200)^2','x',xo,x1);
Irms = (X/(2*%pi))^0.5;
disp('A',Irms,'Irms = ');

//End
```

Scilab code Exa 18.2.b SCR half wave power control circuit

```
clear;
clc;

//Caption:SCR half wave power control circuit
//Given Data
Vs=230;//in V
Rl=200;//in ohm
//Trigger is adjusted so that conduction starts after 60degree of start of cycle
//Instantaneous Current il = (230*2^0.5*sin(a))/200
//It is noted that between 0 to pi/3 SCR voltage equals line voltage and between pi/3 to pi it is zer and for the rest it is equal to line voltage
//Vl = 230*2^0.5*sin(x)
//To find instantaneous power

x0=%pi/3;//lower limit of integral
x1=%pi;//upper limit of integral
X = integrate('(230*230*2*(sin(x)^2))/200','x',x0,x1);
```

```
P = X/(2*3.14);
disp('W',P,'P=');

//End
```

Scilab code Exa 18.2.c SCR half wave power control circuit

```
clear;
clc;

//Caption:SCR half wave power control circuit
//Given Data
Vs=230;//in V
Rl=200;//in ohm
//Trigger is adjusted so that conduction starts after 60degree of start of cycle
//Instantaneous Current il = (230*2^0.5*sin(a))/200

//To find Vrms

//It is noted that between 0 to pi/3 SCR voltage equals line voltage and between pi/3 to pi it is zer and for the rest it is equal to line voltage
xo=0;//lower limit of first integral
x1=%pi/3;//upper limit of first integral
x2=%pi;//lower limit of second integral
x3=2*(%pi);//upper limit of second integral
X1 = integrate('(230*(2^0.5)*sin(x))^2','x',xo,x1);
X2 = integrate('(230*(2^0.5)*sin(x))^2','x',x2,x3);
Vrms = ((X1+X2)/(2*%pi))^0.5;
disp('V',Vrms,'Vrms=');

//End
```

Scilab code Exa 18.3 SCR Relaxation Oscillator Phase control Circuit

```
clear;
clc;

//Caption:SCR Relaxation Oscillator Phase control
    Circuit
//Given Data
C=0.1;//in microF
V=60;//in V
Vb=32;//in V
Vh=10;//holding voltage in V
Ih=100;//in microA
c=45;//conductance angle in degree
cd = 360 - c;//angle in which capacitor will get
    charged
td = (cd/360)*(1/60);//in ms

//if the anode voltage is positive,the SCR will fire
     when vc=32V
vc=32;//in V
//let time constant = t = R*C
//vc-Vh = (V-Vh)(1-exp(-td/t))
t = -td/log(1-((vc-Vh)/(V-Vh)));
disp('sec',t,'time constant = ');
R = t/C;//Resistance in K
disp('K',R*1000,'R=');


//end
```