```
//example 8.7(b)//
clc
//clears the screen//
clear
//clears all variables//
close
//closes all existing files//
disp('By interchanging  the connections of waveforms A and B with
respect to earlier one. Q output will be at logic 0 state as long as
waveform A leads waveform B in phase. In this case, on every occurence
of the leading edge of waveform A(clock input), waveform B(D input) is
in a logic 0 state.')
disp('the rest is shown in diagram')
```