```
//example 8.7(a)//
clc
//clears the screen//
clear
//clears all variables//
close
//closes all existing files//
disp('A positive edge triggered D flip flop, as shown in figure can be
used for the purpose. Waveform A is applied to the D input and waveform
B is applied to the clock input. If we examine the two waveforms, we
will find that, on every occurence of leading edge of waveform B,
waveform A is in logic 1 state. Thus, the Q output in this case will
always be in a logic 1 state')
disp('the rest is shown in diagram')
```