```
//example 8.6(a)//
clc
//clears the screen//
clear
//clears all variables//
close
//closes all existing files//
disp('When the ENABLE input is HIGH, the upper AND gate is enabled
while the lower AND gate is disabled. The outputs of upper and lower
AND gates are D and logic 0 respectively. They constitute inputs of the
NOR gate whose output is D''. The Q output is therefore D')
```