

```
//example 3.5(a)//  
//3 input to exor//  
clc  
//refreshes all variables//  
clear  
//clears the screen//  
disp('in the figure output of first gate is exor of A and B. output of  
second gate is exor output of earlier two gates where A B C are inputs  
to the system')  
//result//
```