

```
//example 3.3//  
clc  
//refreshes all variables//  
clear  
//clears the screen//  
disp('in the figure output of first gate is AB and output of second  
gate is CD output from the third gate is multiplication of output of  
earlier two gates which come out to be ABCD where A B C and D are  
inputs to the system')  
//result//
```