```
//example 3.13//
clc
//clears the screen//
clear
//clears all existing variables//
disp('The NAND gates are used in the circuit are open collector gates.
Paralleling of the two NAND gates at the input leads to a WIRE AND
connection. Therefore the logic expression at the point where the two
outputs combine is given by the equation (AB)''.(CD)''. Using
Demorgan''s theorem (AB)''.(CD)''=(AB+CD)''. The third NAND is wired as
an inverter. Therefore the final output can be written as : Y = AB +
CD')
```