

```
//example 1.9(b)//
clc
//clears the screen//
clear
//clears already existing variables//
disp('when one of the logic input of 2-input NOR gate is 1, then irrespective
of the other input, the output comes out to be 0. In fact, a NAND gate is
disabled or inhibited if one of its inputs is connected to logic 1')
disp('Y=0')
disp('here the output of Y is 0 irrespective of input of A')
```