```
//example 1.7(a)//
clc
//clears the screen//
clear
//clears already existing variables//
disp('when one of the logic input of 2-input NAND gate is 0, then irrespective
of the other input, the output comes out to be 1. In fact, a NAND gate is
disabled or inhibited if one of its inputs is connected to logic 0')
disp('Y=1')
```